General Purpose 1-bit

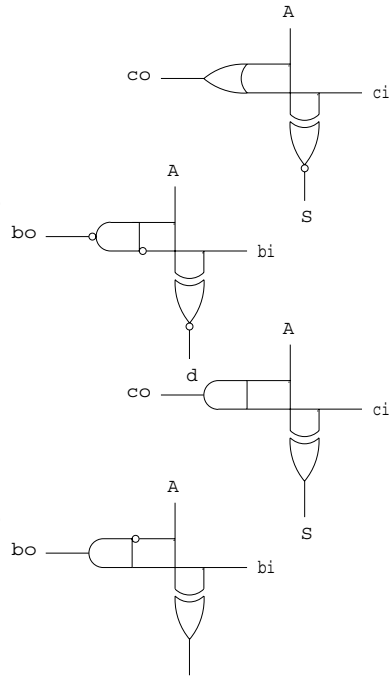
1. Incrementer
2. Decrementer
3. 1/2-Adder
4. 1/2-Subtracter

A	ci	S	co
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	1

A	bi	d	bo
0	0	1	1
0	1	0	1
1	0	0	0
1	1	1	1

A	ci	S	co
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A	bi	d	bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



$p=0=\bar{t}$
$q=1$
$r=1=t$

t=1

$p=0=\bar{t}$
$q=0$
$r=1=t$

$p=1=\bar{t}$
$q=0$
$r=0=t$

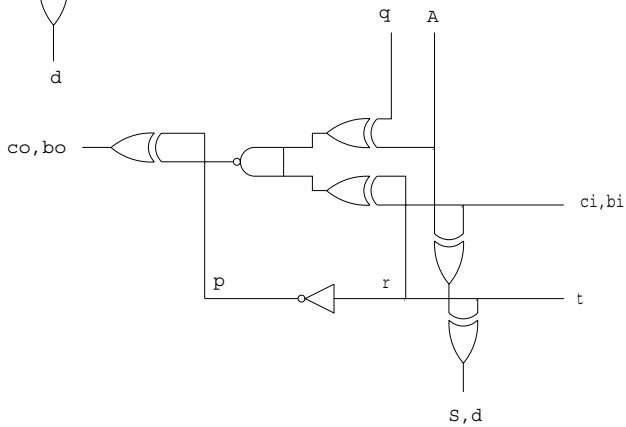
t=0

$p=1=\bar{t}$
$q=1$
$r=0=t$

Instruction

q	t
1	1
0	1
0	0
1	0

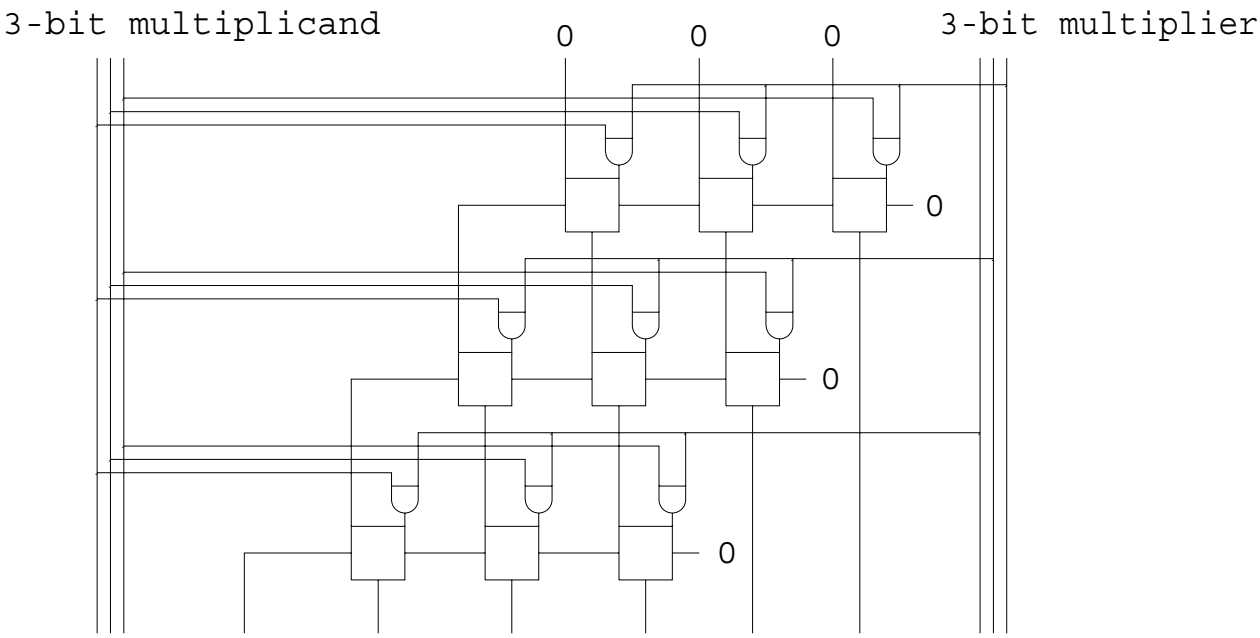
Selected Function



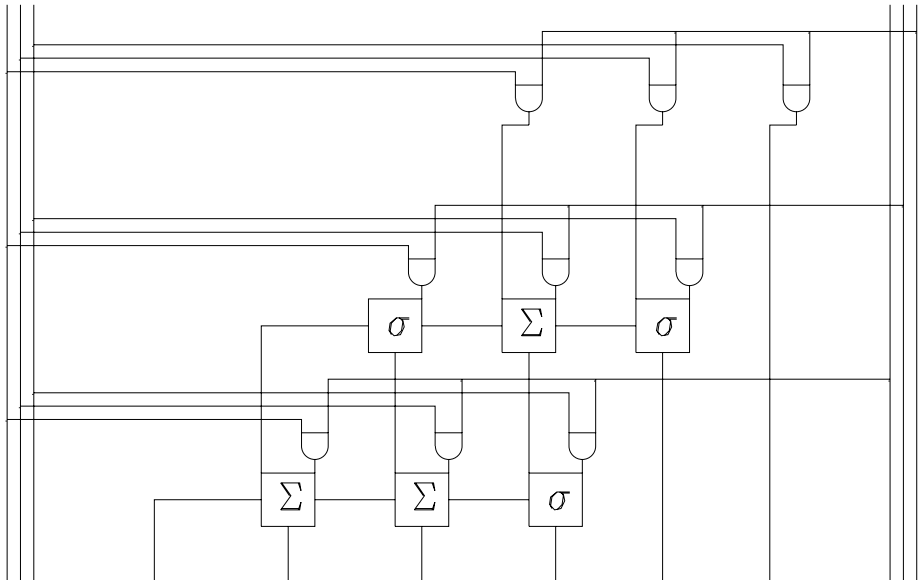
GP1BAU

3x3=6 bit PARALLEL MULTIPLIER

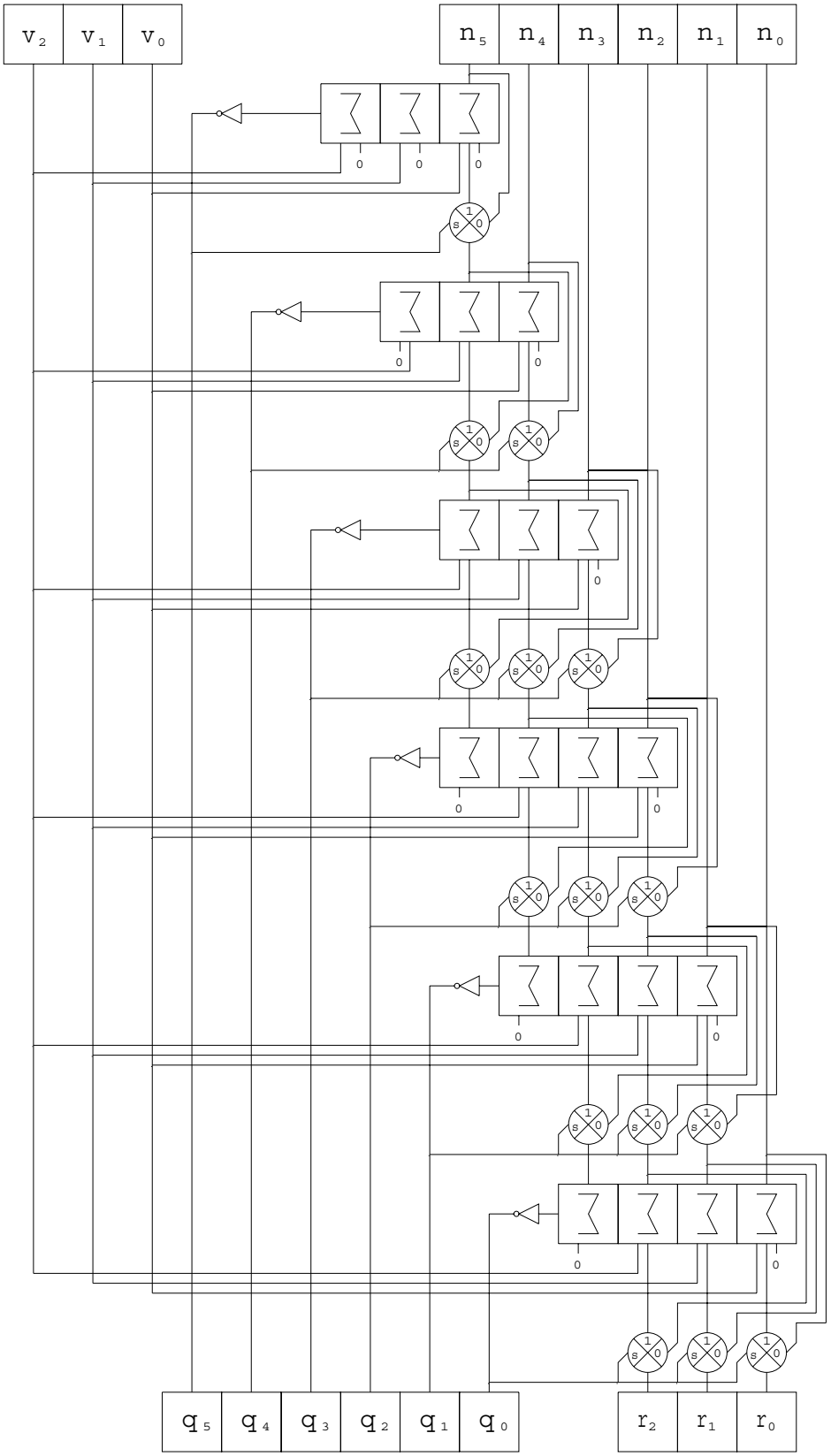
Regular Architecture



Minimal Architecture

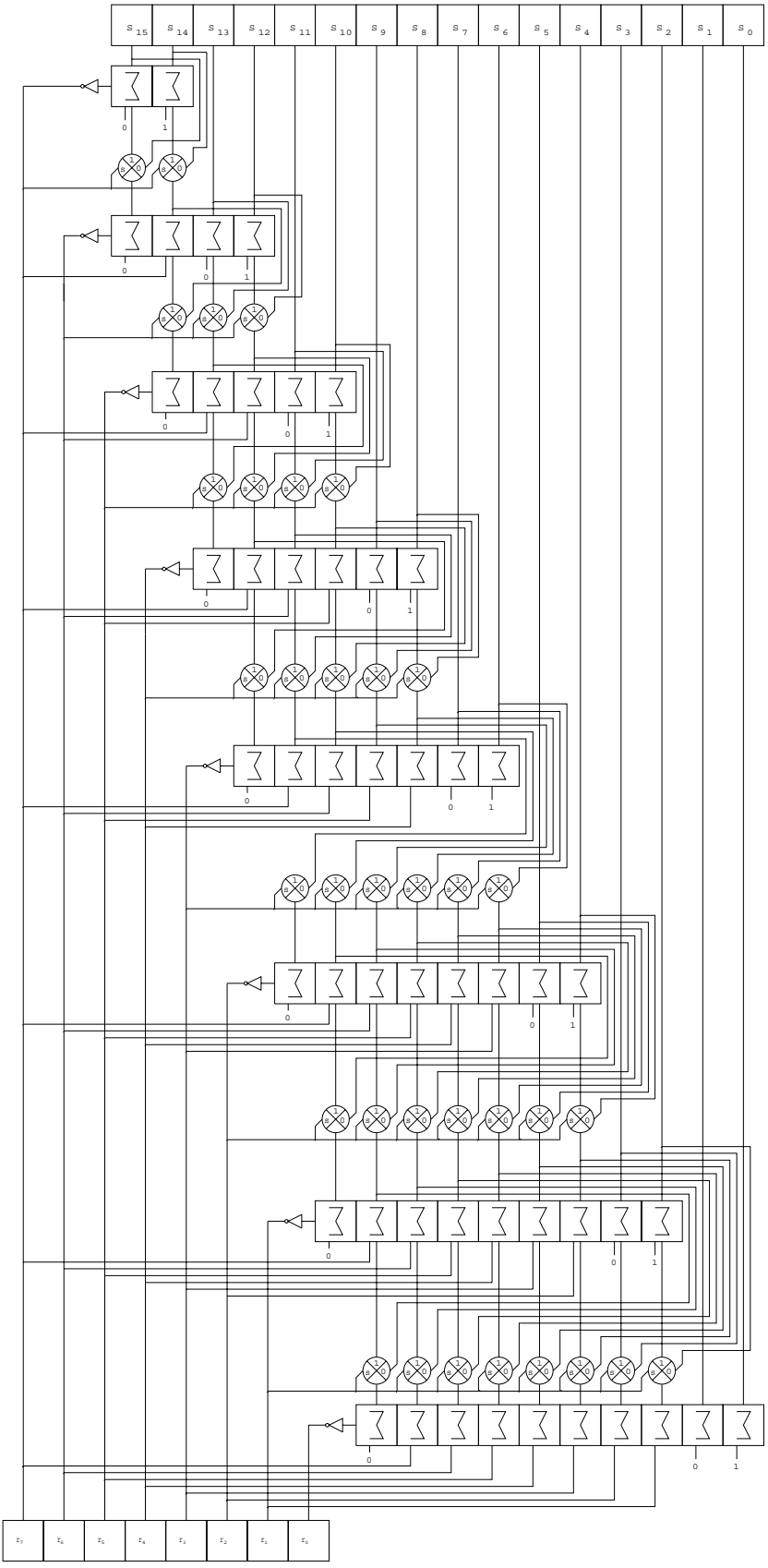


6-bit product



6-bit dividend, 3-bit divisor, 6-bit quotient divider

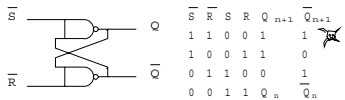
DD6DR3Q6



16-bit to 8-bit parallel square-rooter

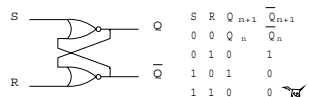
Elements of Sequential Circuits

NAND Flip-Flop



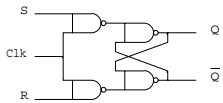
$\overline{S}$	$\overline{R}$	S	R	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0	0	1	1
1	0	0	1	1	0
0	1	1	0	0	1
0	0	1	1	Q_n	$\overline{Q}_n$

NOR Flip-Flop

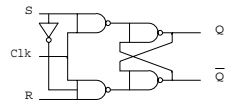


S	R	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	Q_n	$\overline{Q}_n$
0	1	0	1
1	0	1	0
1	1	0	0

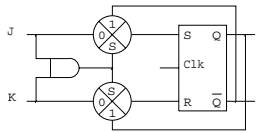
Gated Flip-Flop



SOC (Set overides Clear)

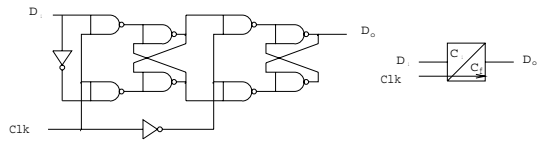


J-K Flip-Flop (Race problem)

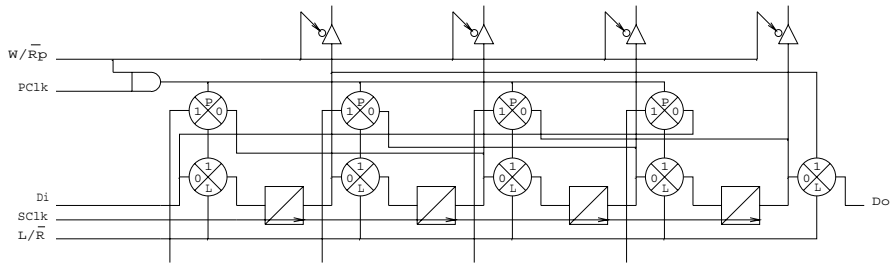


J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Master/Slave Data Flip-Flop

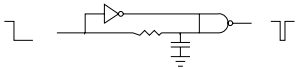


Parallel Outputs

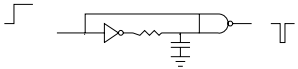


Parallel Inputs

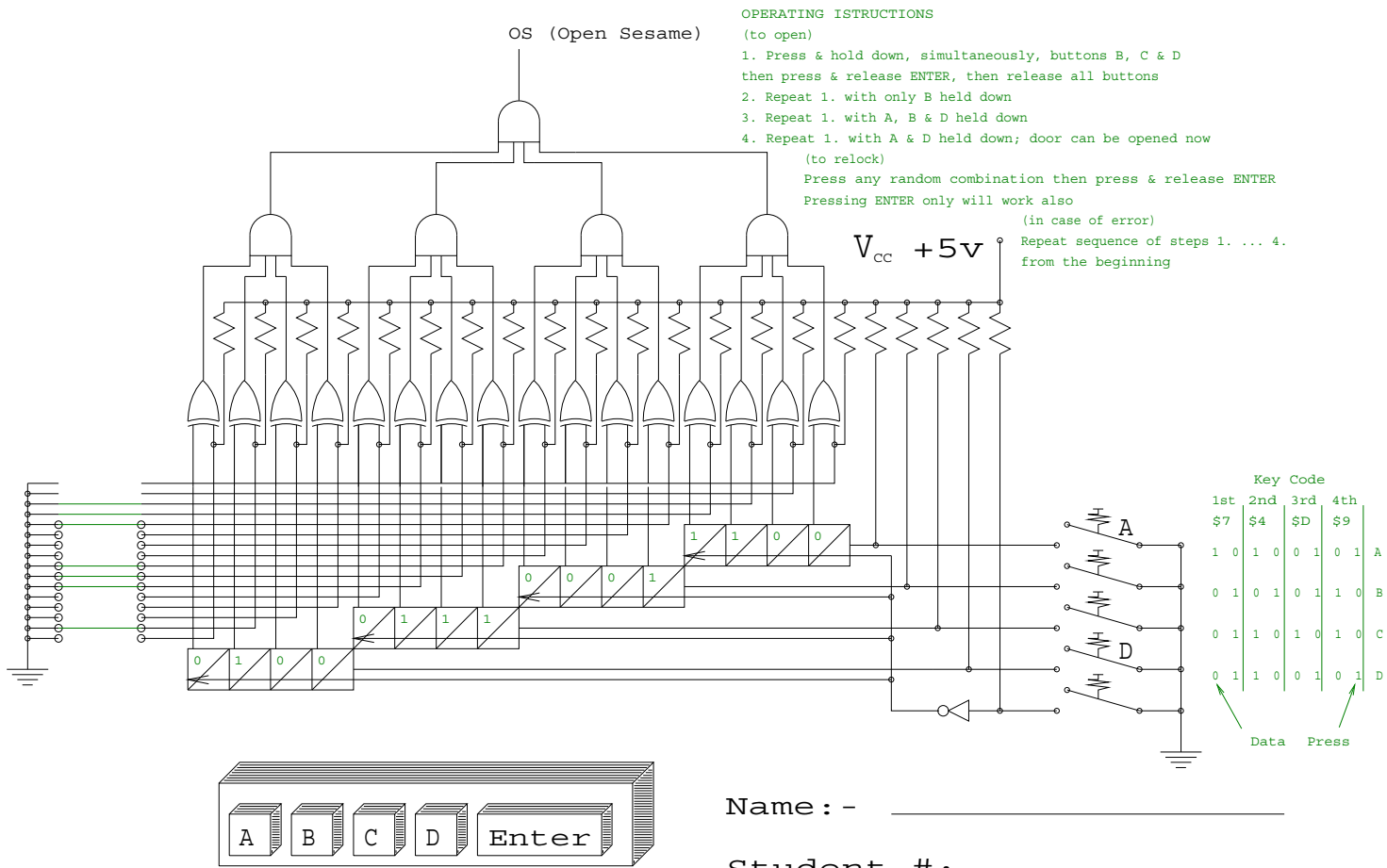
Low going falling edge trigger



Can it be done with NOR-gates?



Low going rising edge trigger



Name:- _____

Student #:- _____

DOORLOCK