Virtual Memory

Tabish Syed
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Virtual and Physical Memory

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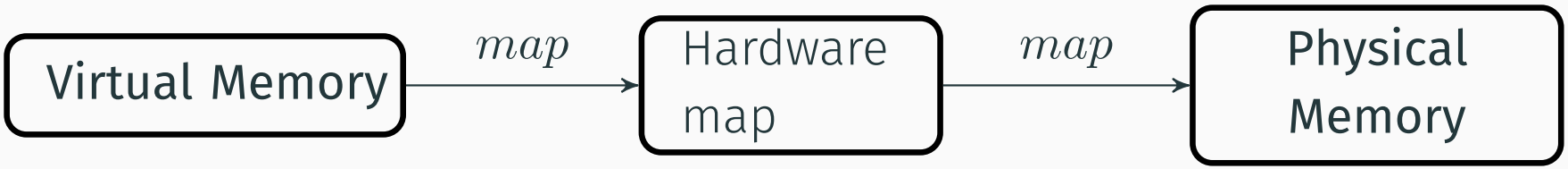

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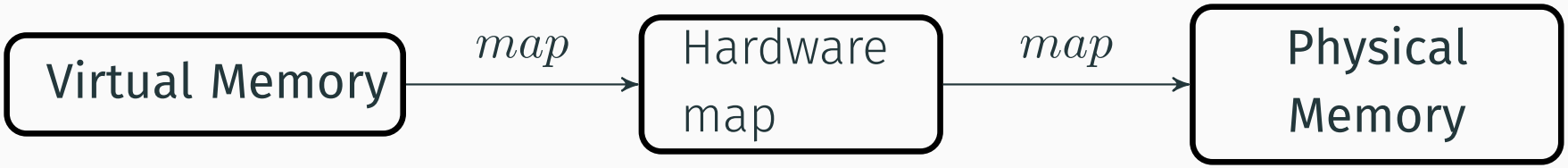

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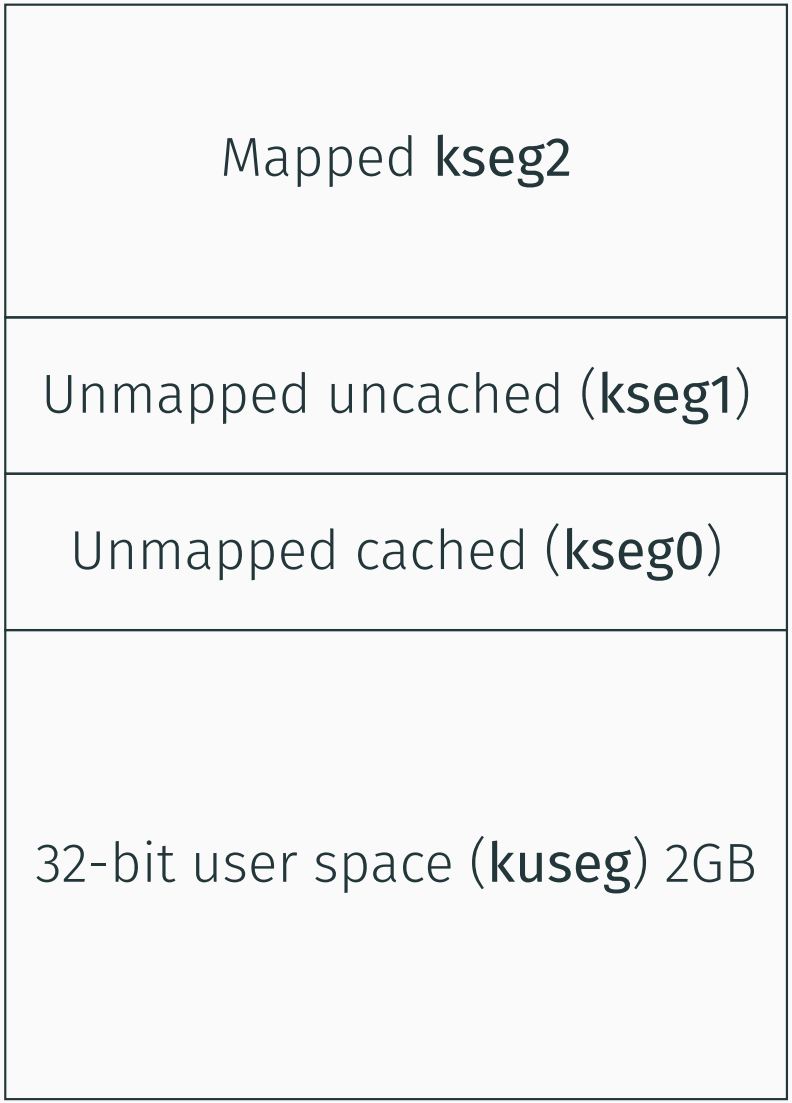
- Memory Translation Hardware Translates virtual address to physical address.
- Each *process* is protected from other running processes.
- OS(software) can decide where each process goes in the physical memory.

Virtual Memory Layout

MIPS Virtual Memory Map



32 Bit MIPS memory map.

MIPS Virtual Memory Map

- kuseg: (`0x000 000 - 0x7fff ffff`) User segment is the lower 2 GB of the 32-bit address space. These addresses are allowed only in user mode. Mapped to physical memory by (Memory Management Hardware/Unit)MMU

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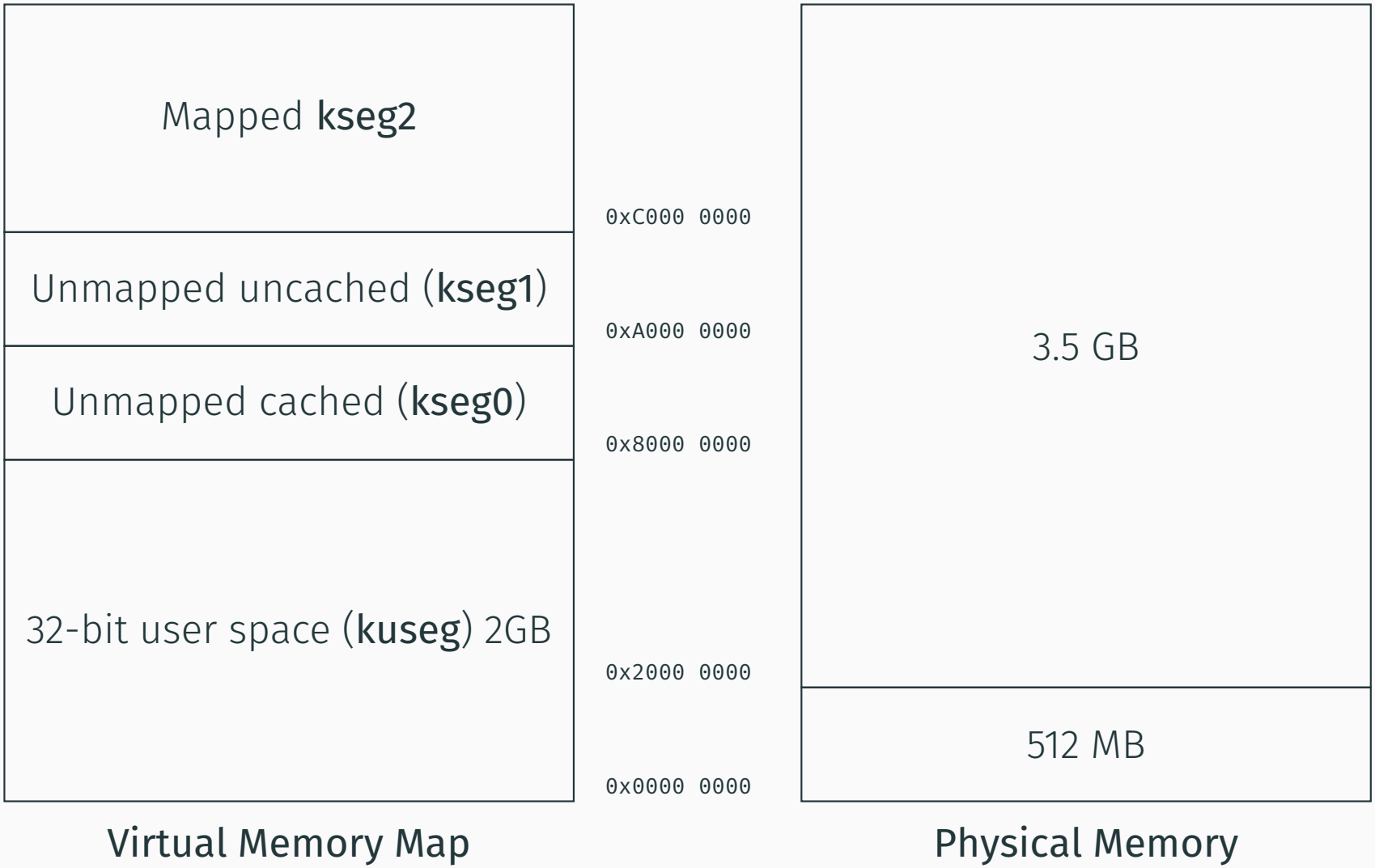
- **kseg2**: (`0xc000 000 - 0xffff ffff`) This 1 GB is only accessible in kernel mode. Mapped to physical memory by MMU

MIPS Virtual Memory Map



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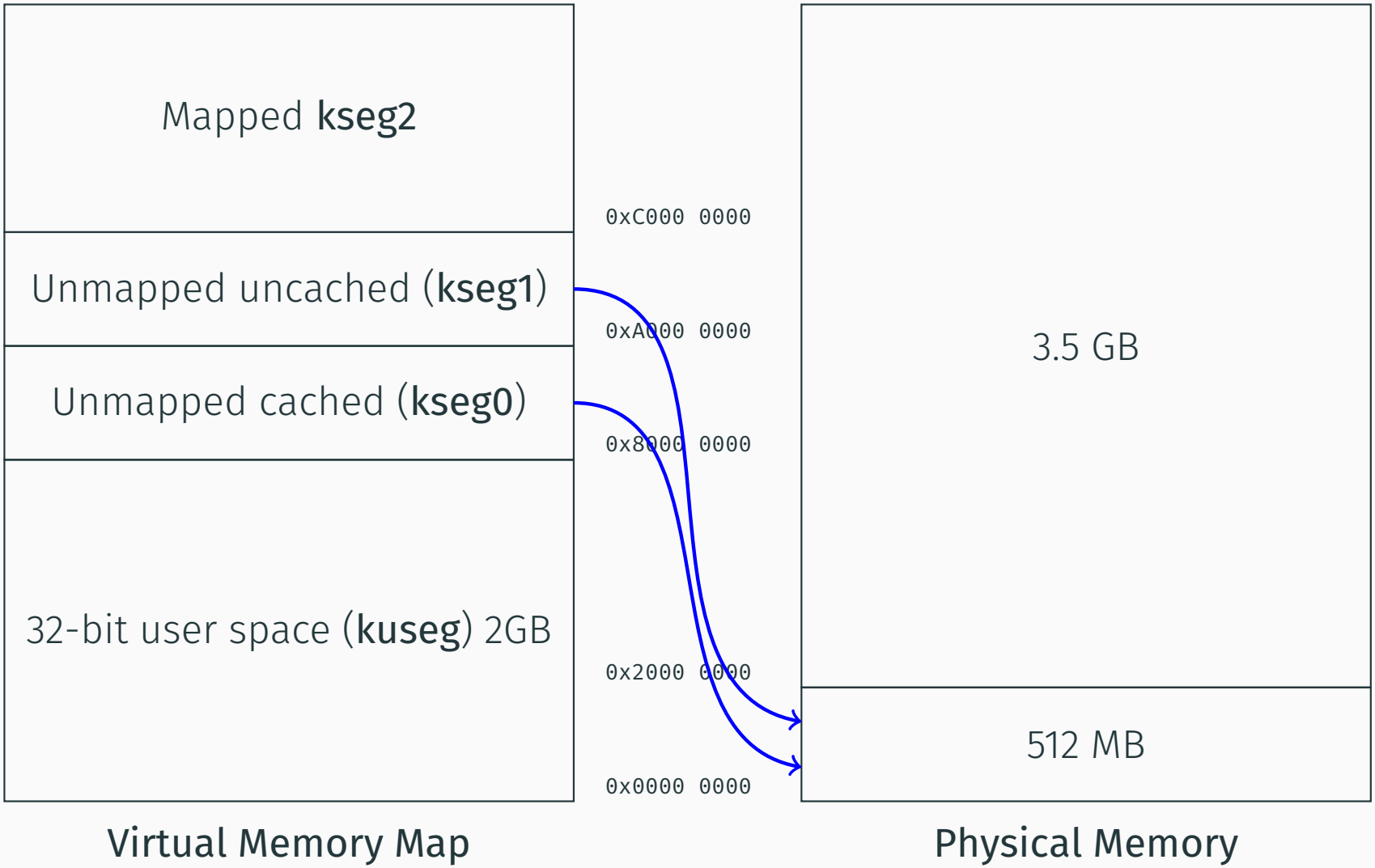

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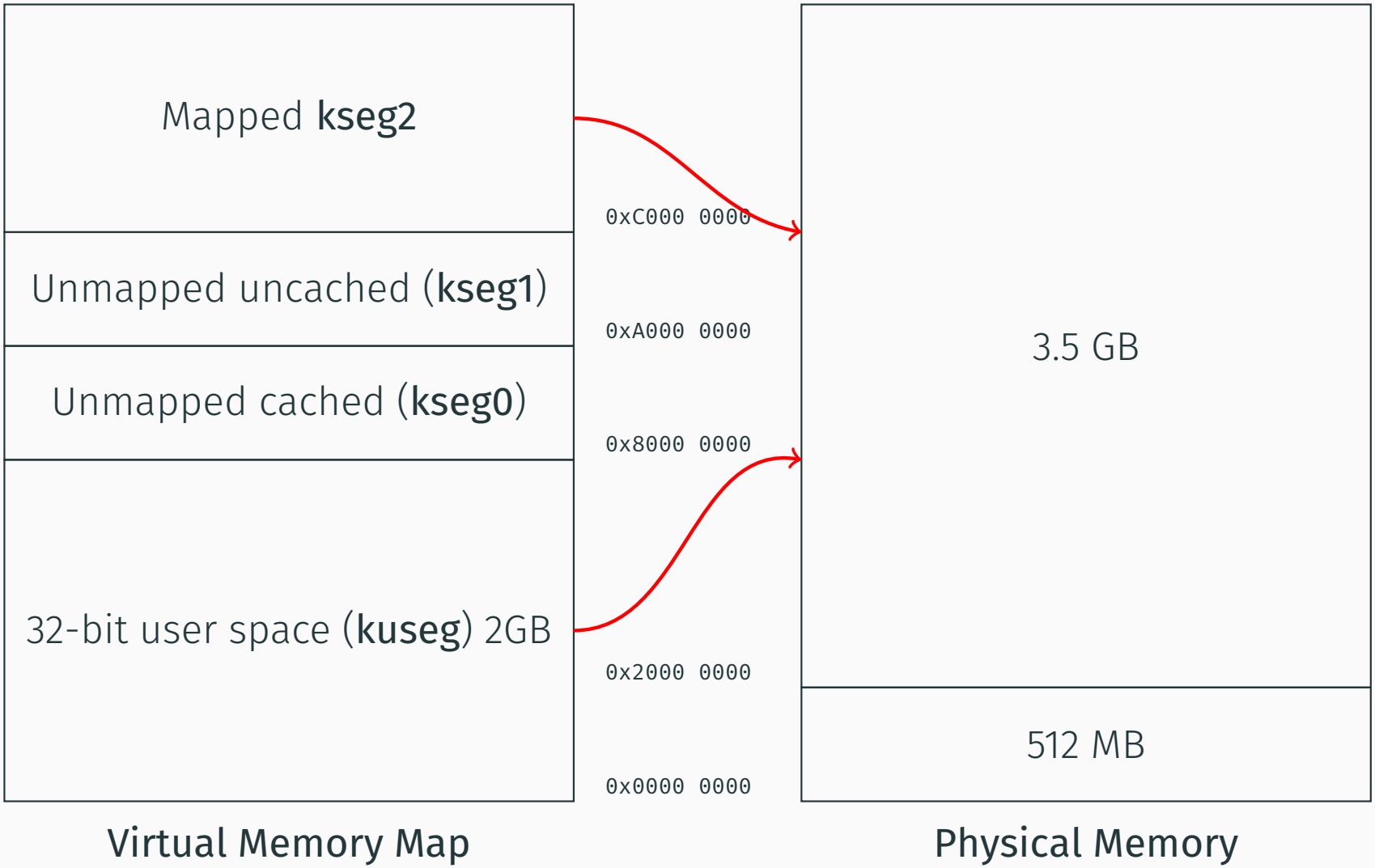

Kernel and User Segments

Privilege level of a program

- **User Privilege:** In User mode program addresses above 2GB ($MSB = 1$) are illegal. Additionally, some instructions, like some CPU control instructions, are illegal.

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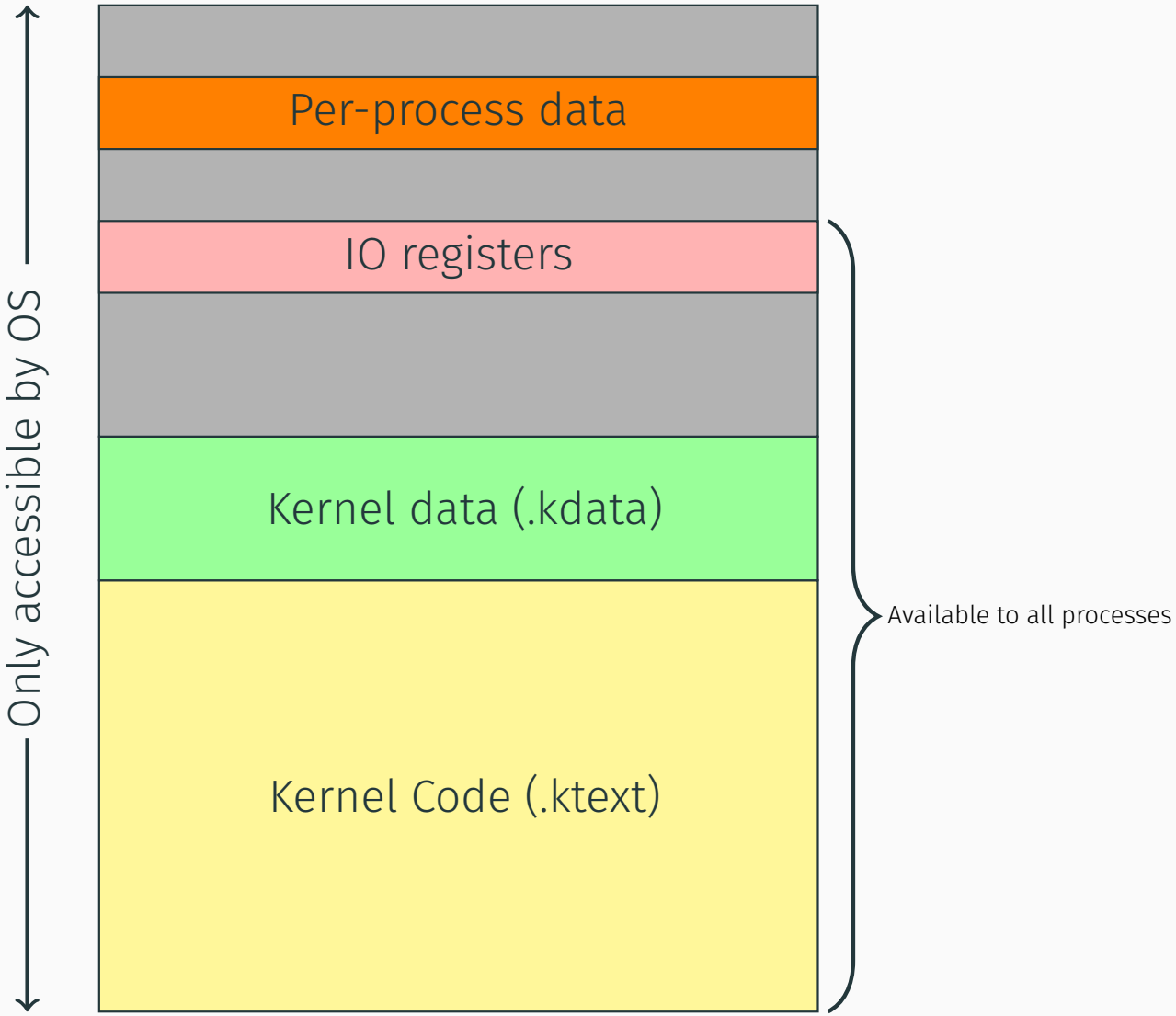
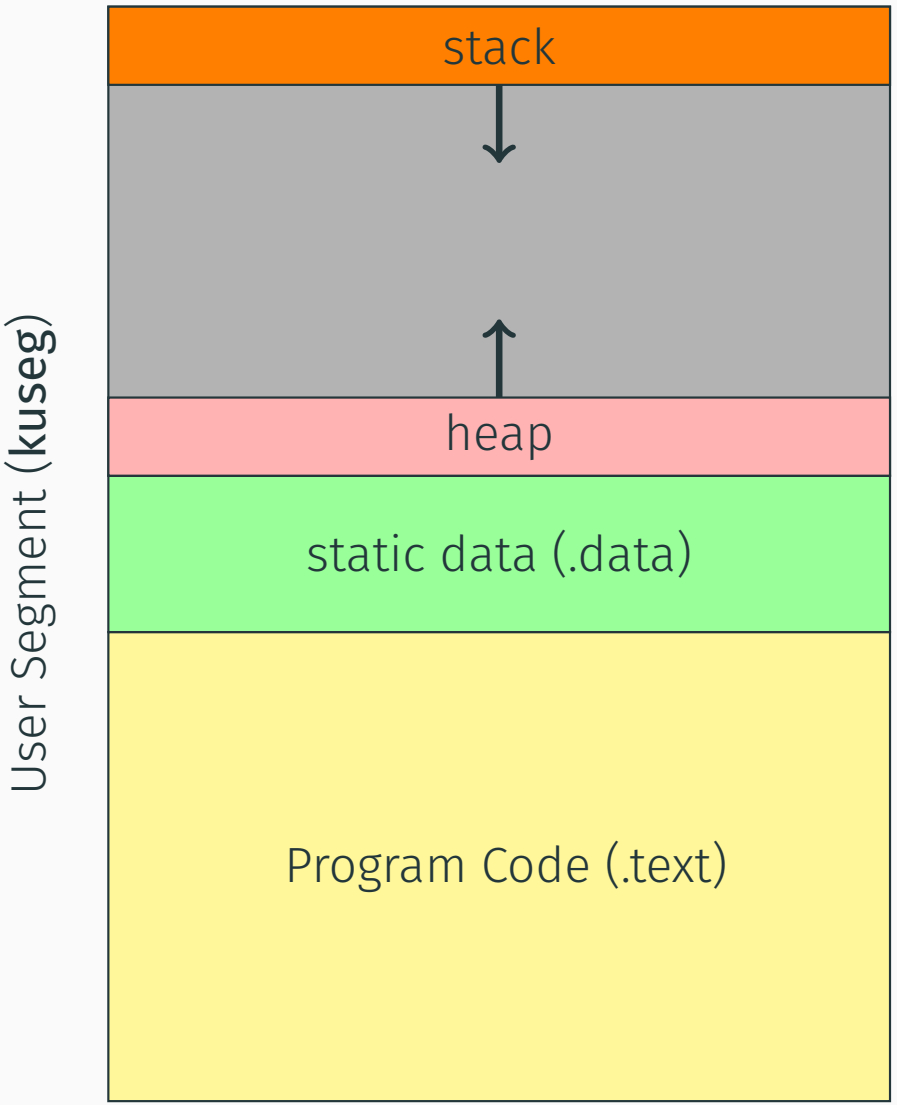
- **Kernel Privilege:** In this mode a program can do anything. Generally OS runs in this mode.

Kernel and User Segments



Kernel Segment.

Kernel and User Segments



User Segment.

Mapping To Physical Memory

Virtual to Physical Address Mapping

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- Mapping also allows OS to discriminate and therefore protect different parts of memory.
- The Kernel part of a processes address space is shared by all processes and therefore maps to fixed location.

Hardware Memory Translation

Memory Translation hardware should achieve the following:

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- **Relocation**: The Memory translation system allows a program to run anywhere in physical memory.
- **Protection**: Programs with user level privilege can only access the *kuseg* segment. Regions of memory can be write protected.
- **Demand Paging**: Programs can run as if all the memory resources they needed were already allocated, but OS actually allocates the space when needed.

Paged Mapping

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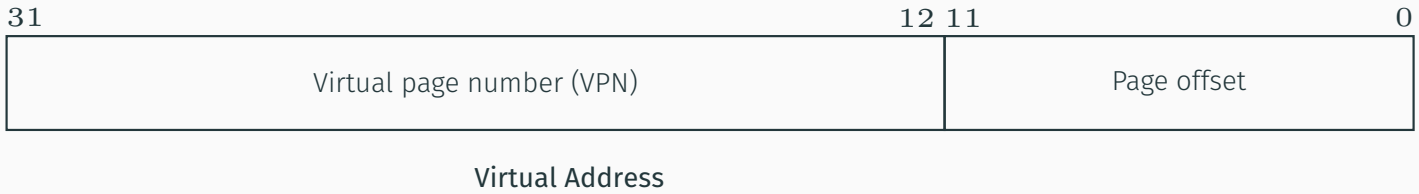
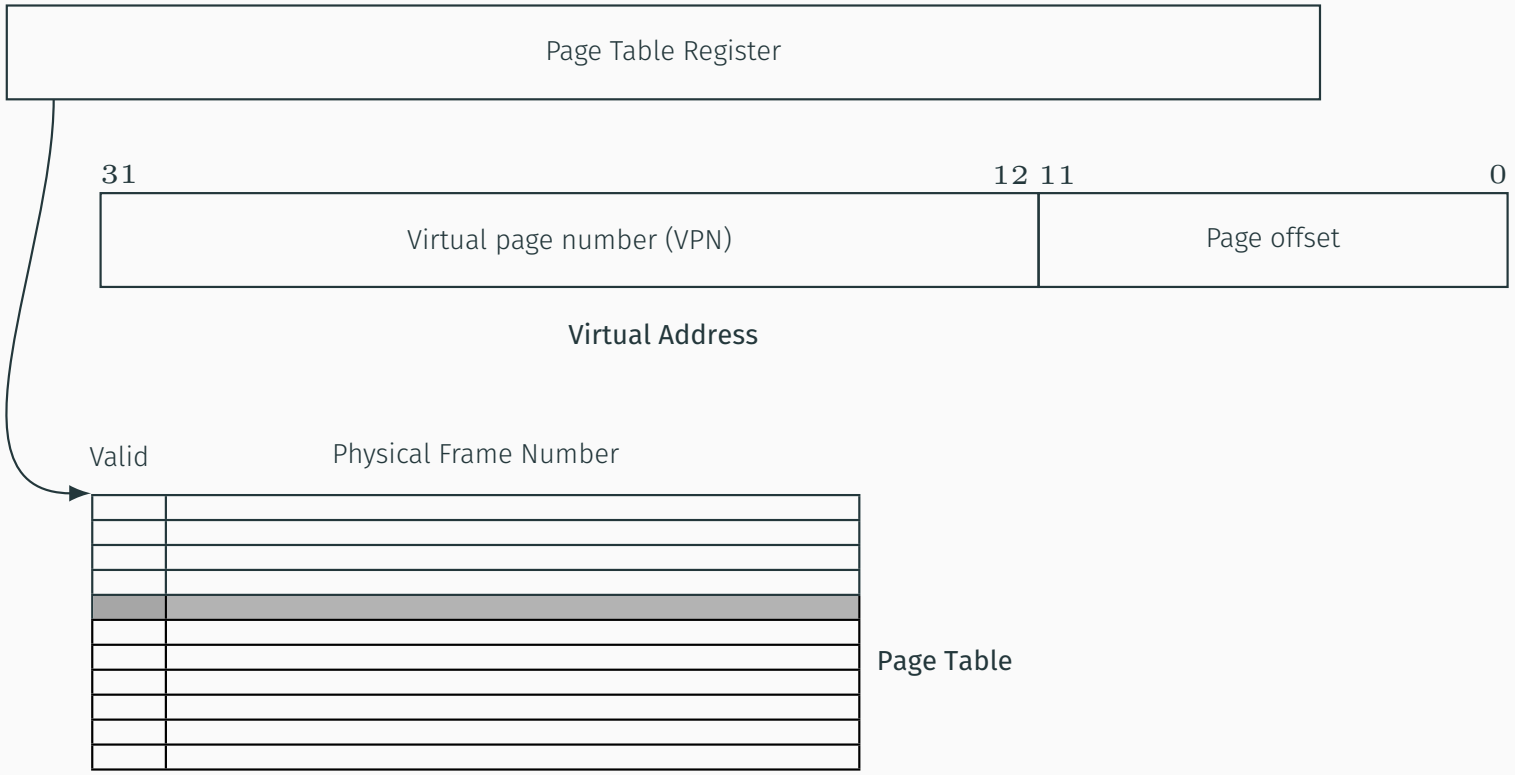
- Mapping translates **virtual page number** (VPN) into **physical *frame* number** (PFN).
- To allow for efficient mapping we maintain a **page table** containing entries for each page.
- To improve translation speed (part of) the page table resides in a fast cache called **Translation lookaside buffer** (TLB) (Which part?).

Paged Mapping



Virtual Address

Paged Mapping



Mapping Virtual Addresses to Physical Addresses

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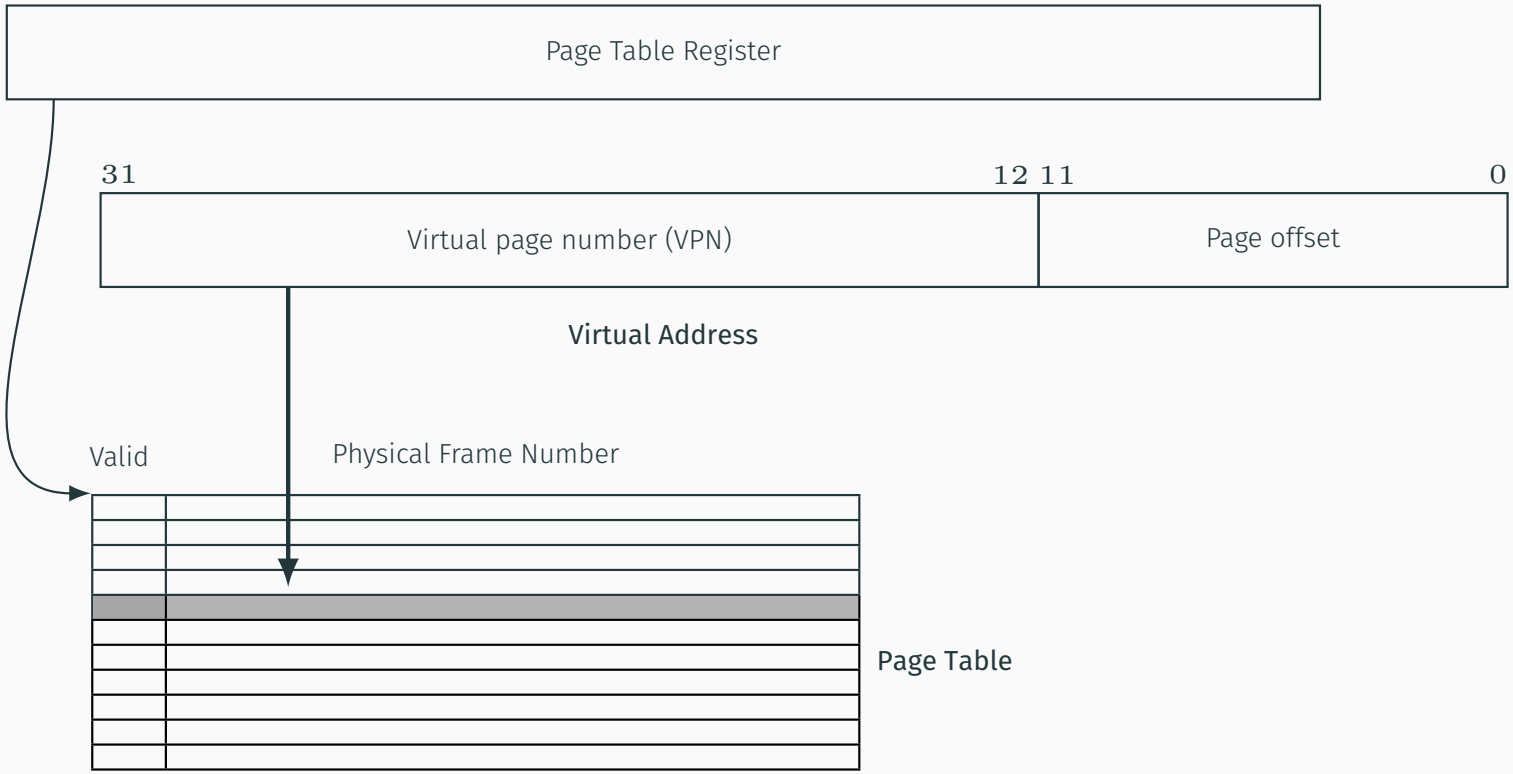

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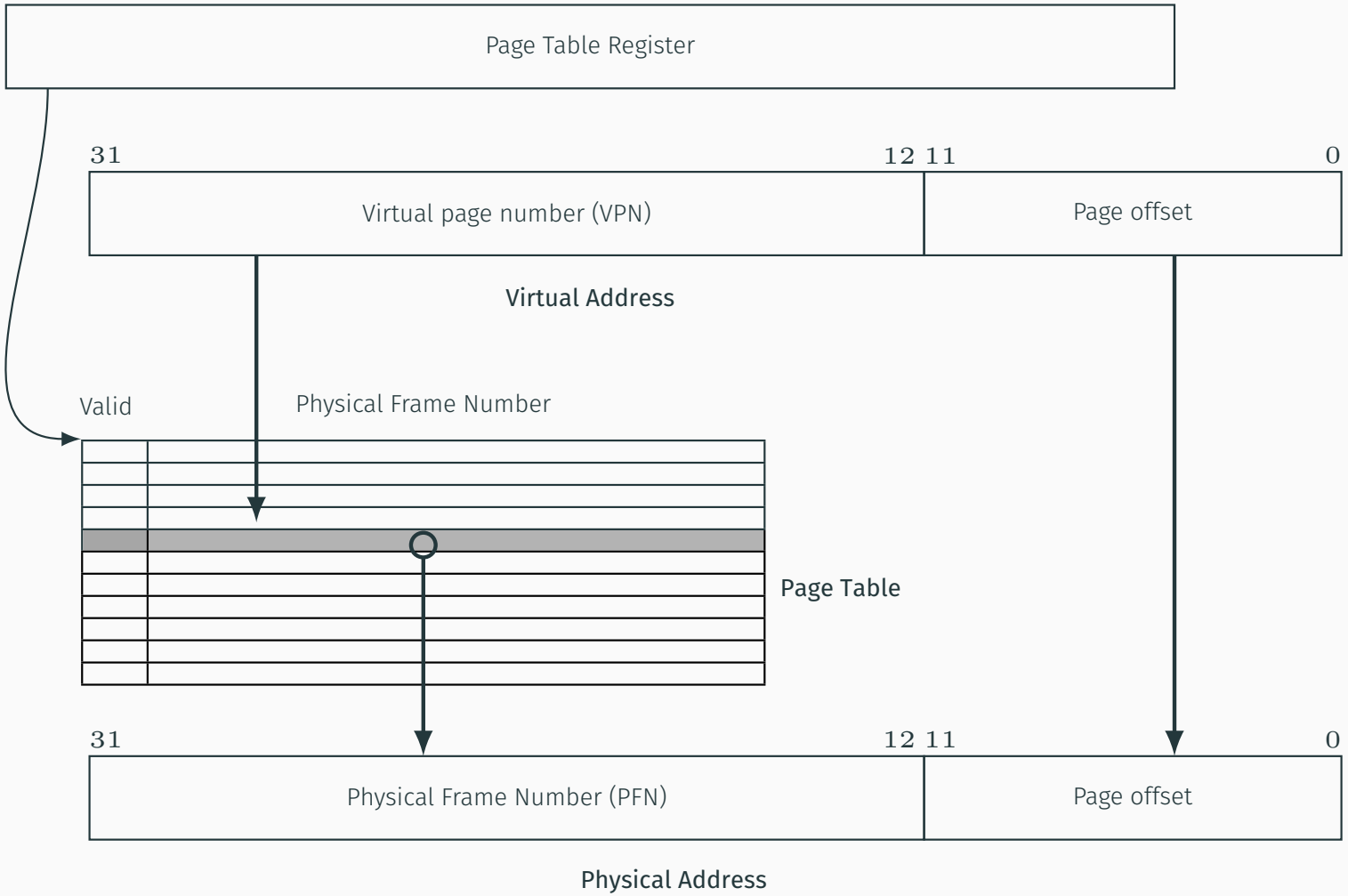

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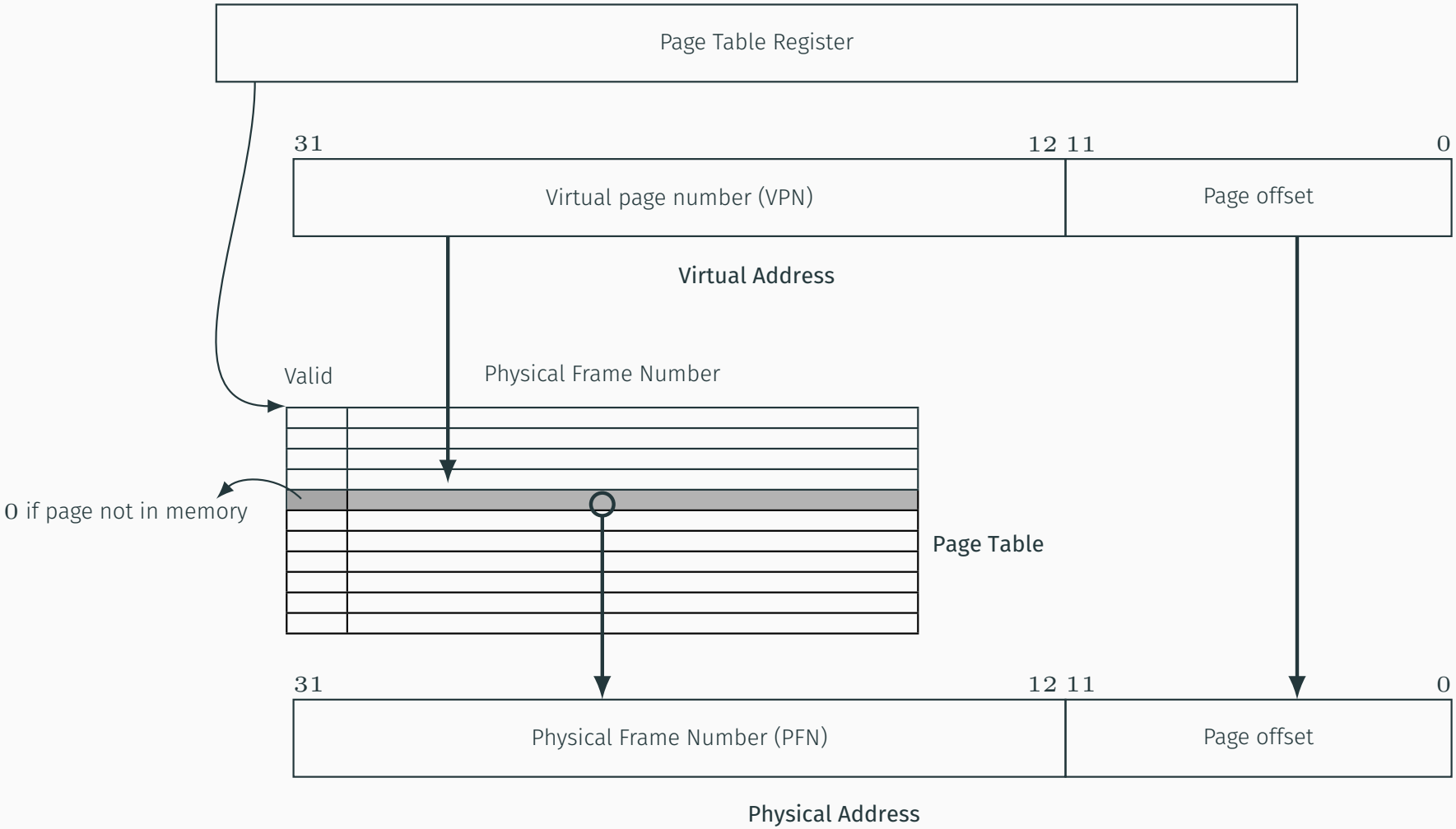

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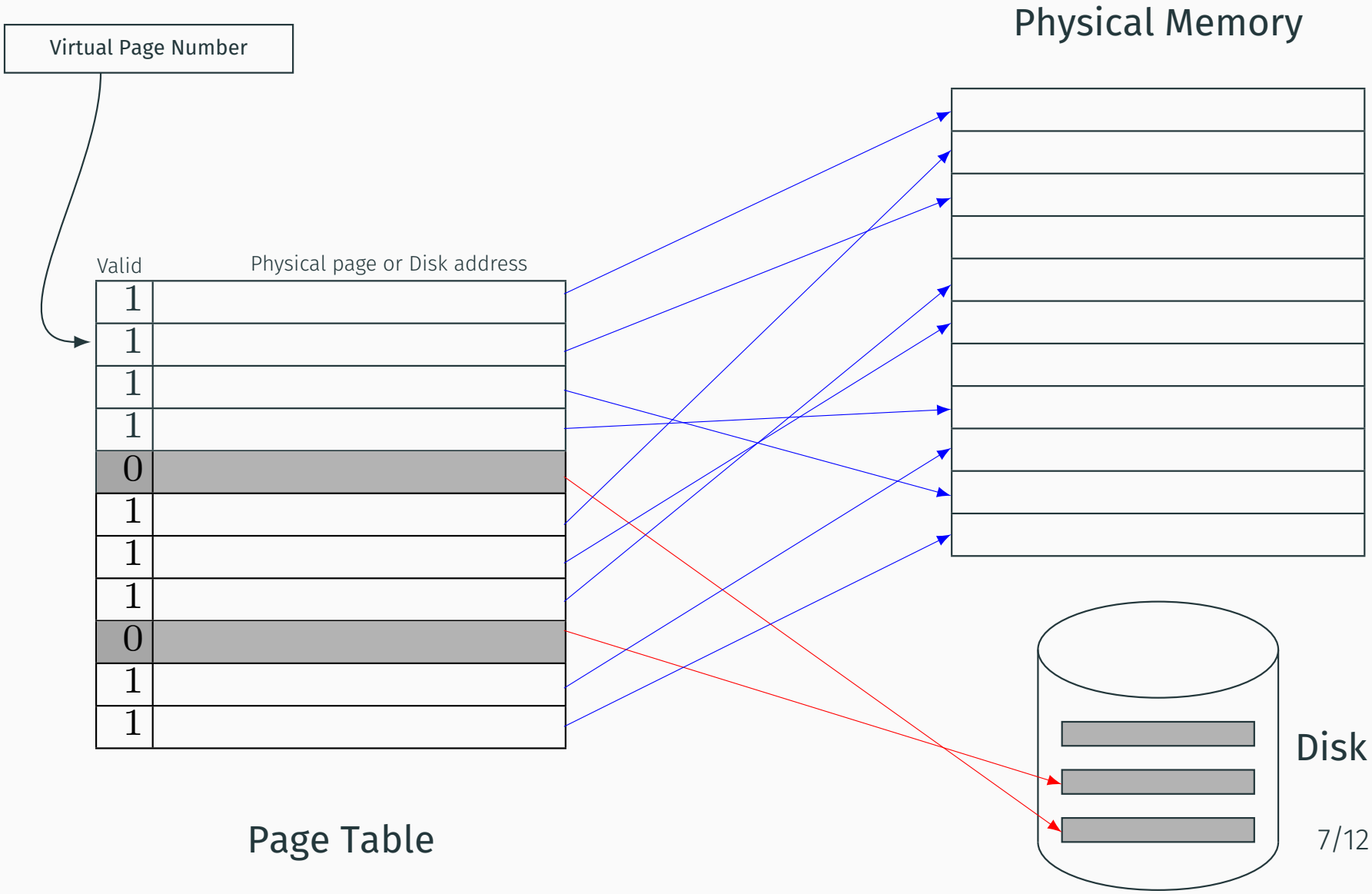

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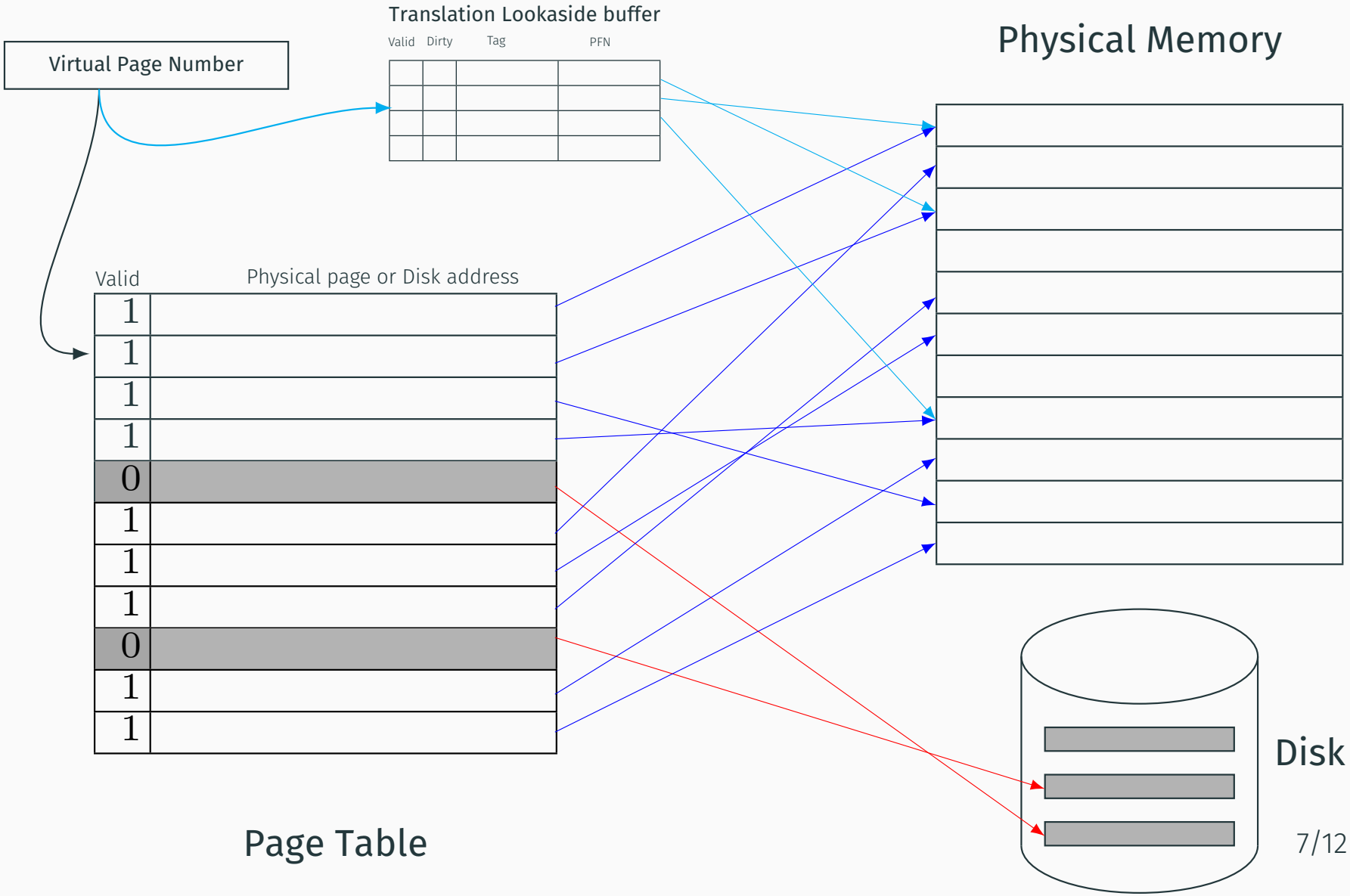
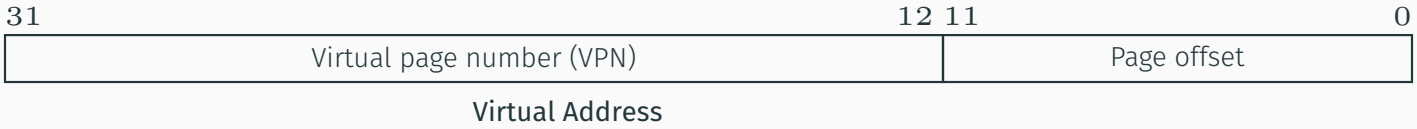


Cache and Virtual Memory



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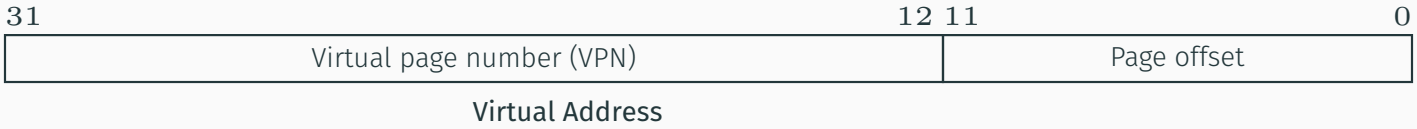

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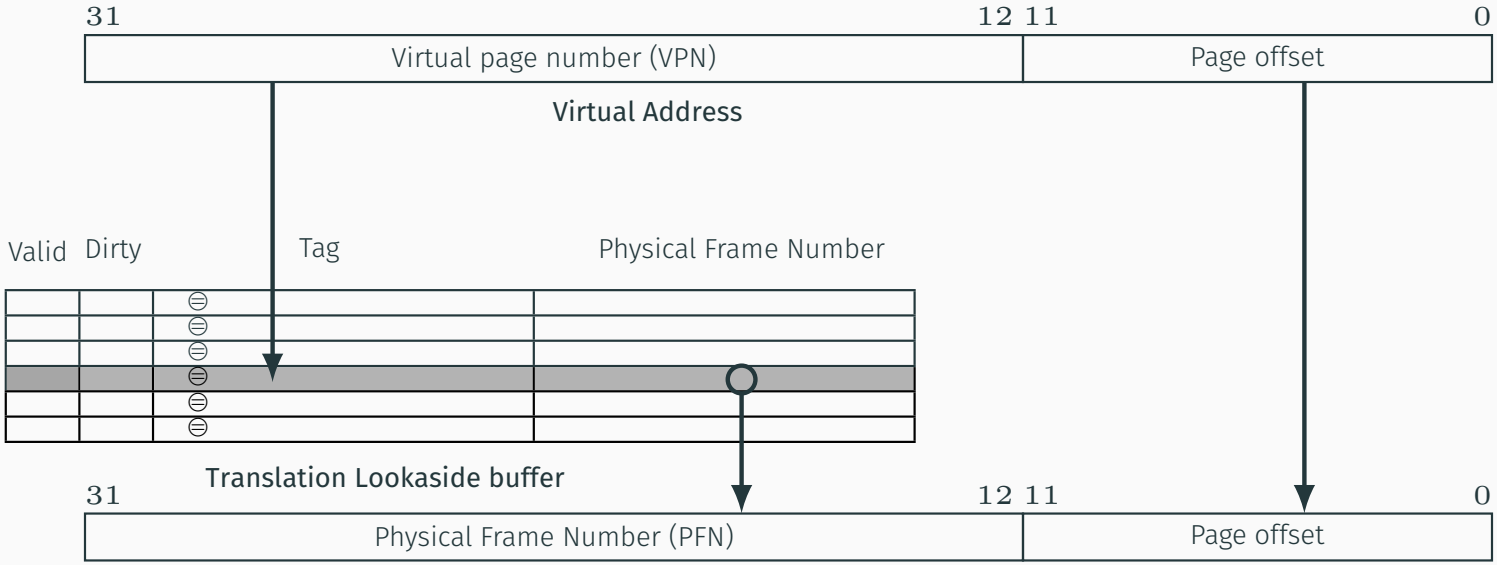

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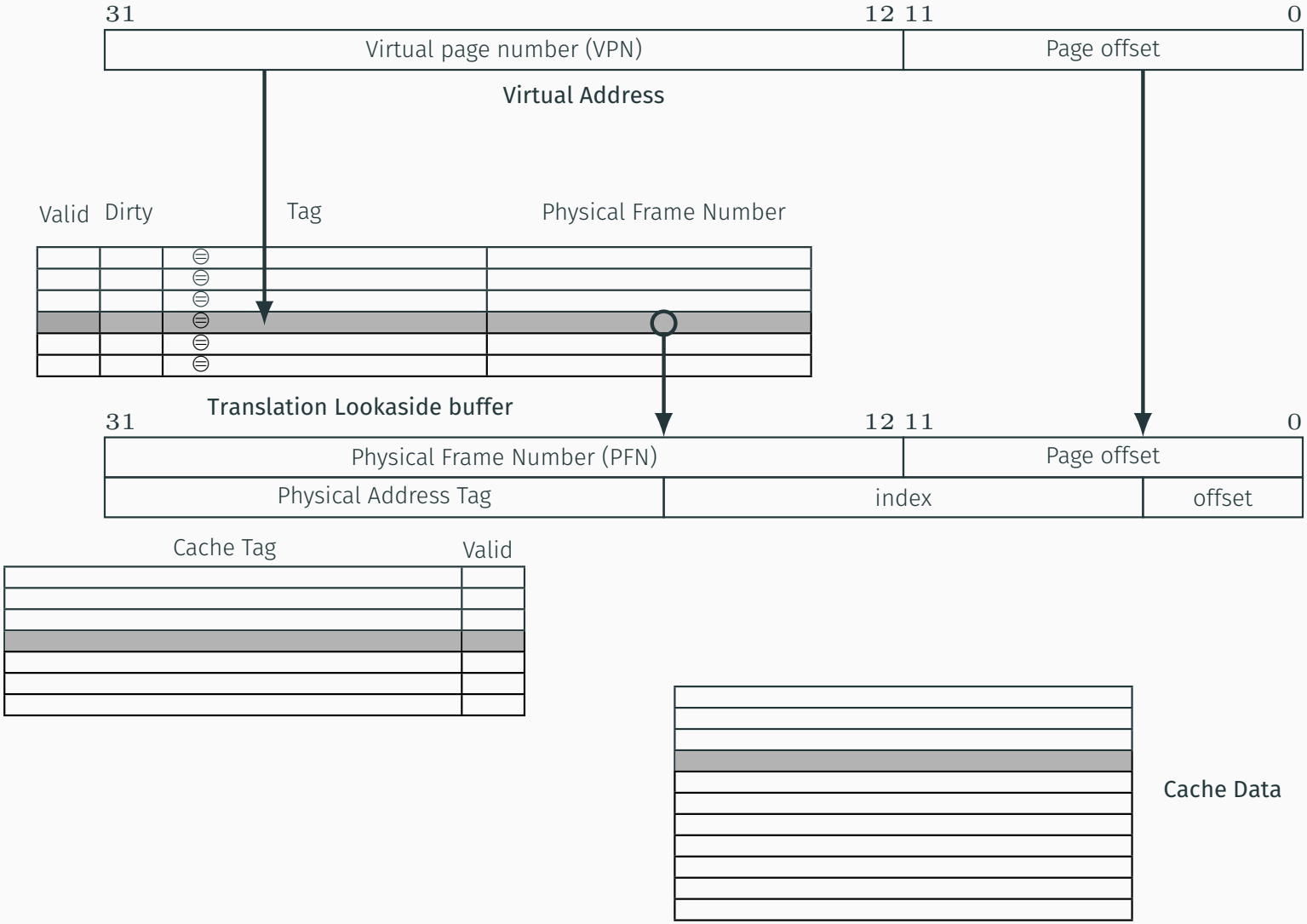

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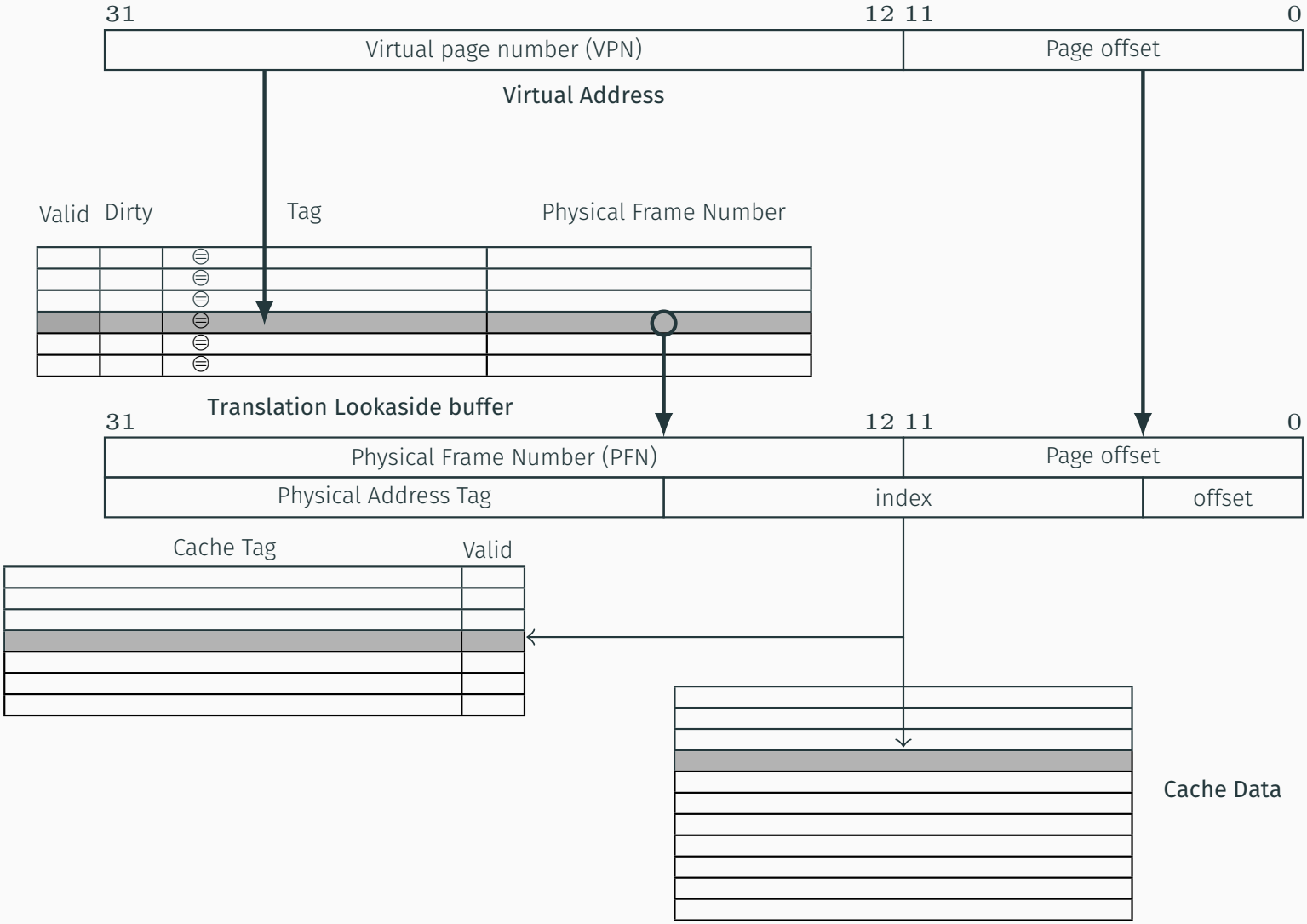

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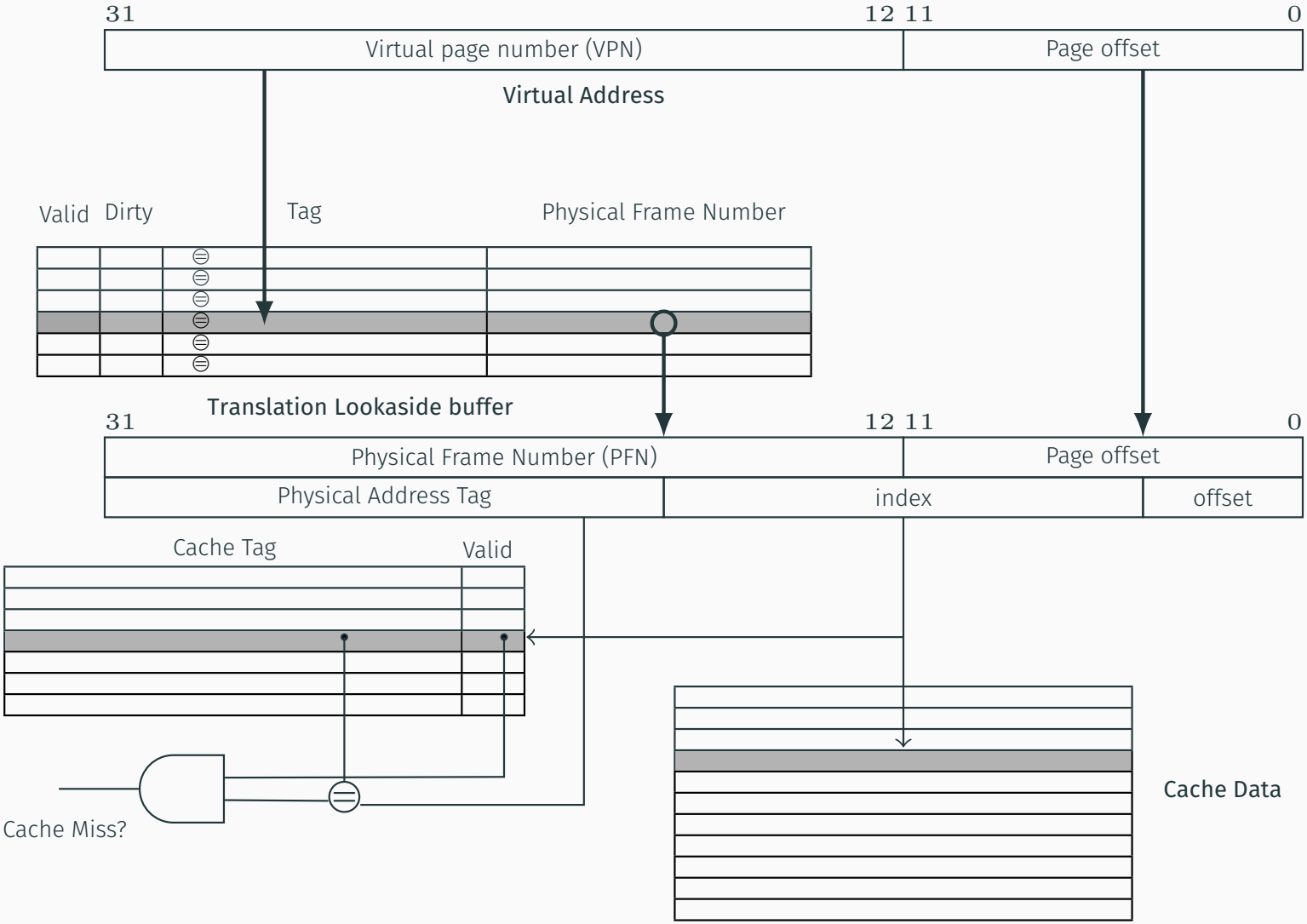

Cache Misses, TLB Misses and Page Faults

TLB	Page Table	Cache
Miss	Hit	Hit

- **TLB** Misses, but entry present in Page Table. Data found in cache.

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TLB	Page Table	Cache
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- **TLB** Misses, but entry present in Page Table. Data not in cache.

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Miss	Hit	Hit
Miss	Hit	Miss
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- **TLB** Misses, followed by page table miss (**Page Fault**). Always followed by **Compulsory Cache miss**

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- Cannot have entry in **TLB** if page is not in memory.

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Summary

Caches

- Cache Block(Line)

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- Memory Page

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Caches

- Cache Block(Line)
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Summary

Caches

- Cache Block(Line)
- Cache Miss
- Cache Size: 32-64 B

Virtual Memory

- Memory Page
- Page Fault
- Page Size: 4KB

Summary

Caches

- Cache Block(Line)
- Cache Miss
- Cache Size: 32-64 B
- N-Way set associative

Virtual Memory

- Memory Page
- Page Fault
- Page Size: 4KB
- Fully Associative