lecture 6
Sequential circuits 2
- T flipflops, counters and timers (finishing last lecture)
- register array
- RAM

January 27, 2016

TODAY: from flip flops to RAM

T flip flop (toggle)

Assume falling edge triggered.

Q: What does this circuit do?
Assume falling edge triggered flip flops.
Qi is the clock input for flip flop i + 1.
i increases from left to right.

Correction of incorrect claim made from last lecture (see below).

D flip flop ("rising edge triggered")

By putting the inverter on the first D latch, we would make Q change its value on the rising edge of the clock. There is no advantage to this, so for simplicity we will always work with falling edge triggered.

Q: What does the circuit do?

A: 0 7 6 5 4 3 2 1 0

Timer (count down)

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Sequential circuits 2
- T flipflops, counters and timers
- register array [recall what a register is]
- RAM

January 27, 2016
In MIPS, there are 32 registers, and each is 32 bits. There is no significance to the fact that the number of registers is the same as the number of bits per register.

Suppose the variables \(x, y, z\) are stored in registers. How to read \(y\) and \(z\)? How to write the result into \(x\)?

Recall idea from last lecture:

- Use sets of D flip flops (register) to store numbers \(A\) and \(B\).
- Compute \(A + B\) using the circuit shown, and write the new value back into \(B\).

For the next slide, we will rotate \(A\) and \(B\) so they are horizontally oriented and have 32 of them (not 2), each 32 bits (not 8).

Sometimes we write as follows (inputs on left, outputs on right).
WriteEnable
ReadReg1
ReadReg2
WriteReg
WriteData

ReadData1
ReadData2

address
data
control

} types of signals

For larger memory arrays, the multiplexor design is not physically feasible. You need $N^2$ wires coming out. But the side of the square array only grows with $N$.

An alternative approach? ... somehow have only $2N$ wires, namely a read and a write wire for each column.

Consider what happens for each of the $N^2$ flip flops. All flip flops in a row (column) share the same horizontal (vertical) wire.

MemWrite
clock C
RowSelect

There is a problem, however. The ReadData line reads from all rows simultaneously, which is not allowed. We need to select one. How?

Tri-state Gate (not a logic gate)
- also known as a 'tri-state buffer'
- output can have values 0, 1, or none (voltages are low, high, or zero)

The idea is that only one row is connected to the ReadData line.

We have been thinking of reading or writing an entire row.

We would not allow MemRead and MemWrite to both be 1 (not shown in circuit). Also, sometimes neither would be 1.

Let's next select only a single row and column.
e.g. Consider 8 chips with $2^{16} \times 2^{15}$ bits on each chip.
This defines $2^{31}$ bits per chip or $2^{31}$ bytes (2 GB).

Announcements

- Quiz 1 and yellow stickies

- Quizzes: who writes in Arts 145? (70 seats)
  Quiz 2 A-H
  Quiz 3 I-P
  Quiz 4 I-P
  Quiz 5 R-Z
  Quiz 6 R-Z

- Assignment 1 posted ~next Monday, download 'logisim'
  (there will be a demo on class on Monday)