lecture 22

Input / Output (I/O) 4
- asynchronous bus, handshaking
- serial bus

Mon. April 4, 2016

"synchronous" bus
= clock based
(system bus clock is slower than CPU clock)

"asynchronous" bus
= not clock based
(distance between sender and receiver is too great for accurate timing i.e. physical variability)

Communication between device controllers and devices often is asynchronous (e.g. USB - universal serial bus)

"Handshaking": one method for an asynchronous bus

sender initiated
- e.g. printer controller to printer

receiver initiated
- e.g. parallel port for (pre-USB) printer

It can be initiated by source (sender) or by destination (receiver).

Handshaking can work for shared buses too.

Example:
- "parallel port" for (pre-USB) printer

Handshaking can work for shared buses too.

However, note that there needs to be a mechanism to ensure that only one device can write to bus at one time.

For example, we saw solutions to this problem already when we discussed the (clocked) system bus, e.g. dedicated BR/BG or IRQ/IACK lines including daisy chaining. We will see another scheme later in the lecture when we discuss USB.

Note that address, data, and control may be many bits each.
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Parallel bus
- multiple lines
- data needs time to stabilize

Serial
- one line
- data doesn't stabilize (next slide)

Serial bus e.g. USB
- one line only!
- data doesn't stabilize, but rather it travels down the wire like a wave
- sender and receiver both have clocks (but not synchronized and may have very different frequencies)

Sender and receiver must agree on a signal pulse duration (greater than their clock pulse duration (typically \(\text{GHz}\)) i.e. lower signal pulse frequency than clock pulse frequency).

How to send bits? (simple model -- one byte)

\[
e.g. \quad 56,000 \text{ bit/sec (band)}
\]
\[
1.5 \text{ M bit/sec}
\]
\[
100 \text{ M bit/sec}
\]
\[
500 \text{ M bit/sec (USB 2.0)}
\]

Sender samples every \(T\) (duration of pulse) until byte is read (samples in middle of pulses)

Detecting Errors - parity bit
Add an extra bit to a byte so that the total number of 1's is even (called 'even parity').
The original ASCII was 7 bits with the 8th bit used for parity.
We can detect only if there was an odd number of errors.
Note the difference between detection and correction. Parity bits do not allow us to correct the error(s). We would need to send the message again.
Modern methods of 'error correcting codes' use abstract algebra (theory of finite fields)
UART - universal asynchronous receiver transmitter
- I/O controller and I/O device typically both have one
- contain shift registers
- can do parity checking too

USB - universal serial bus
- A: plug into computer (host)
- B: plug into device

USB controller ("host")
- polls the USB device ("speak when spoken to")
- interrupts the CPU

USB packets
Fields of a packet include:
- synch - used to synchronize the clocks of controller and device
- PID (packet ID) -- what type of packet is it? (r/w? handshake?..)
- address -- which device is it for? (each device gets a number when it is plugged in)
- data
- error correction info

A USB bus can have up to 127 devices on it.
Despite the tree structure, the system behaves as a bus. All devices and host see all signals.

"Plug and play" (plug and pray)
- USB host senses a new device, so it interrogates it ("who is the new device who just plugged in?")
- USB host then sends info about th device to the OS
- OS loads the driver from disk (or tries to get on www) device manufacturers give drivers to Microsoft, Apple

EXERCISE:
Why can't you just rip out your USB stick from your computer? Why do you have to formally 'eject' it?

On Windows 7
Control Panel -> Hardware -> Device Manager -> USB controllers

when I plug in my printer, this one appears
Optical Mouse
- image frame is ~20 x 20 pixels
- camera capture is 1500 frames/sec
- image processing software finds best shift between images

Analog video port
I/O controller (graphics card) has an A/D converter

Digital video port
HDMI (high definition multimedia interface - carries audio too)
DVI (digital video interface)

Announcements
A3: - TA email are on page 1 of A3.pdf
- grading scheme is posted on public web page

A4: MIPS register conventions abused in my evaluate function. See discussion board.
- pick up your quizzes

TODO (not on final exam)
Wed: thinking about graduate school?
next Mon: Quiz 6 + more on caches
next Wed: JVM