QUIZ 5 Introduction to Computer Systems COMP 273
Mon. March 21, 2016 Professor Michael Langer

LASTNAME: _____ FIRSTNAME: _____ ID: _____ GRADE: _____/4

Instructions:

You are allowed one crib sheet. Once you finish, turn your paper over and wait for the end of the quiz.

Questions:

1. Consider a computer with a MIPS processor, a page size of 2^{10} bytes (1 KB), a TLB with 2^{12} entries, a main memory (RAM) with 2^{31} bytes (2 GB), and an instruction cache with 2^{15} blocks having 8 words each.

   For each question below, you must show how you obtained your answers. You will get 0 if you only give the correct answer.

   (a) How many bits are used for each virtual page number?

   ANSWER: 22. Each page index uses the lower 10 bits for indexing and the remaining bits (32-10 = 22) are used for the virtual page number.

   We gave 0.5 point instead of 1, if you reasoned that 31-10 = 21.

   (b) Which bits (from 0 to 31) of the virtual address are used for the TLB index ?

   ANSWER: Bits 10 to 21. The VPN from Q1 is bits 10 to 31. The lower 12 of these are used for the TLB index, hence bits 10 to 21.

   We have 0.5 point instead of 1‘, if you had 12 bits in your answer (but the wrong 12).

   (c) How many bits are used for each physical page number (for a page in RAM)?

   ANSWER: 21. There are 2^{31} bytes in physical address space. Each page again is 2^{10} bits. Hence there are 31-10 = 21 bits needed to address each physical page.

   (d) How many bits are in the tag field of each line of the cache?

   ANSWER: 11. Each block in the cache has 2^5 bytes and so 5 bits (namely 0 to 4) indicate the 'byte offset' within each block. The next 15 bits (namely 5 to 19) of the physical address are used to index which block. This leaves 31-20 = 11 bits for the tag.

   We gave 0.5 point, if you mentioned that 5 bits were needed for byte offset within a block.