ments between the circuit and detector must be minimised. A radical improvement is presently obtained by eliminating the parasitic beam due to the reflection at the back surface of the circuit (Fig. 1). For this purpose, the circuit plane is slightly tilted off the incident beam axis and an iris diaphragm is used for spatial filtering. The beam of interest (reflected at the front surface of the circuit) still propagates in the right direction owing to the use of a cat's eye configuration with the incident beam focused on to the metallic layer.

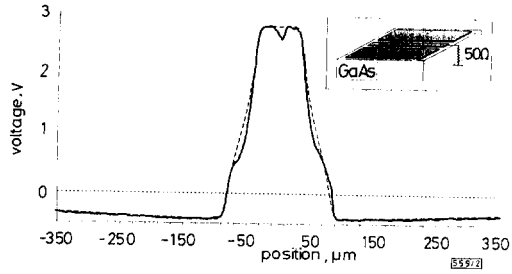

Fig. 2 *Evolution of potential difference between two faces of 50Ω coplanar line measured (calculated) in direction transverse to electrodes*

——— measurements deduced from current modulation depth $i_{AC}(t)/i_{DC}$
– – – – numerical simulations
Inset: schematic representation of coplanar line, dotted line indicating displacement of probe beam

Measurements and simulations: To validate the method of calibration, measurements were performed on a simple circuit consisting of a 50Ω GaAs coplanar line (inset of Fig. 2). The GaAs substrate was 450μm thick and 70μm wide, and the active electrode was separated by 50μm gaps from the 300μm ground electrodes. No special process was needed for electro-optic sampling. The back surface of the substrate was naturally frosted and the device was simply mounted on an x-y translation stage with a BK7 window. Potential mapping was realised by translating the device in the direction transverse to the electrodes (see inset of Fig. 2). The circuit plane was slightly rotated around this direction to avoid parasitic reflections at the front surface. A continuous readjustment of the beam focus during translation was thus not required in this condition. The translation accuracy was ±1μm. The beam spot size was 10μm at the focal point.

Following the calibration method, the DC and AC components of the detector current were measured simultaneously. The AC component was amplified with a very-low-noise preamplifier (× 28) followed by the lock-in amplifier (× 1025). The DC component was amplified with a lowpass amplifier (selectable gain of 5 or 100). Fig. 2 shows the measured evolution of $i_{AC}(t)/i_{DC}$ when translating the device (full curve). The measurement frequency is 3 GHz and the voltage amplitude is $V_0 = 3.3 \pm 0.3$V. As seen, the noise level is less than 1%. The modulation depth of the photodiode current is $\Delta = 2.4 \pm 0.15\%$ at maximum. As the potential difference between the central electrode and the opposite face of the substrate represents ~86% of the voltage amplitude, we can estimate V_π from $\sim 0.86\pi V_0/\Delta$, which gives $V_\pi = 3.7$kV (±15%).

The 2-D potential distribution was calculated with the Flux-Expert program based on a finite-element model (broken curve in Fig. 2). The finite probe-beam size was simulated by using a convolution of results obtained at different positions with a Gaussian of width identical to the laser beam waist. As seen, there is an excellent agreement between numerical simulations and experimental results. The minor discrepancies are readily explained by weak irregularities of the electrode surfaces as well as residual parasitic reflections of the laser beam. Comparison between experiments and calculations confirms the previous value estimated for V_π, which is not far from that used by different authors (≈ 5 kV).

Conclusion: An electro-optic sampler equipped with a 1.55μm gain-switched laser diode has been developed for precise voltage measurements on high-speed III-V integrated circuits. Using an original method of calibration, we have demonstrated that absolute voltage measurements are feasible by internal probing within an accuracy of ~15%. Still better accuracy (a few percent) is expected with further optimisation of the optical configuration.

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L. Duvillaret (*LAHC, Université de Savoie, Campus Scientifique, 73376 Le Bourget-du-Lac Cedex, France*)

J.-M. Lourtioz (*Institut d'Electronique Fondamentale, URA 22 du CNRS, Université Paris Sud, Bât. 220, 91405 Orsay Cedex, France*)

L. Chusseau (*EMM, Université de Montpellier, Place E. Bataillon, 34095 Montpellier Cedex 2, France*)

References

1 WEIGARTEN, K.J., RODWELL, M.J., and BLOOM, D.M.: 'Picosecond optical sampling of GaAs integrated circuits', *IEEE J. Quantum Electron.*, 1988, **QE-24**, pp. 198–220
2 VALDMANIS, J.: '1THz bandwidth prober for high-speed devices and integrated circuits', *Electron. Lett.*, 1987, **23**, pp. 1308–1310
3 NEES, J., and MOUROU, G.: 'Non-contact electro-optic sampling with a GaAs injection laser', *Electron. Lett.*, 1987, **22**, pp. 918–919
4 WIESENFELD, J.M., and HEUTMAKER, M.S.: 'Frequency response of an internal amplifier in a high-speed integrated circuit measured by electro-optic sampling', *Electron. Lett.*, 1988, **24**, pp. 106–107
5 KARAGANOV, V.L., PORTNOI, E.L., SINYAVSKII, N.M., STAL'NENIS, A.P., STELMAKH, N.M., and CHELNOKOV, A.V.: 'Non-invasive electrooptical measurement of ultrashort electrical signals with the use of a picosecond semiconductor laser', *Sov. Tech. Phys. Lett.*, 1990, **16**, pp. 557
6 TAKAHASHI, T., AOSHIMA, S., TSUCHIYA, Y., SOLLNER, T.C.L.G., and SHEN, J.: 'Improvement of space-dependent sensitivity and absolute voltage measurements in noncontact picosecond electro-optic sampling', *in* SOLLNER, T.C.L.G., and SHEN, J. (Eds): OSA Proc. Picosecond Electronics and Optoelectronics, Vol. 9, 1991, Washington DC, pp. 70–74
7 LI, M.G., CHAUCHARD, A., LEE, C.H., HUNG, H.L.A., SOLLNER, T.C.L.G., and SHEN, J.: 'Two-dimensional field mapping of GaAs microstrip circuit by electrooptic sensing', *in* SOLLNER, T.C.L.G., and SHEN, J. (Eds): OSA Proc. Picosecond Electronics and Optoelectronics, 1991, Washington DC, Vol. 9, pp. 54–58
8 CHUSSEAU, L., BOUCHON, D., DUVILLARET, L., and LOURTIOZ, J.-M.: 'Autocorrelation at 1.3–1.5μm using POM crystal', *Electron. Lett.*, 1990, **26**, pp. 589–590
9 DUVILLARET, L.: 'Echantillonnage électro-optique de circuits intégrés avec lasers à semiconducteurs picosecondes'. Thesis of Paris XI-Orsay University, 1994

Analogue system for eigenvalue computation and sorting based on an isospectral matrix flow

N. Saxena and J.J. Clark

Indexing terms: Analogue computer circuits, Eigenvalue and eigenfunctions, Matrix algebra

An analogue system for the computation of the eigenvalues of symmetric matrices and for sorting lists is described. The computation is based on an isospectral matrix flow. A fully parallel continuous time implementation of the equations is presented. The implementation was simulated using PSPICE, and the results of the simulation are described.

Introduction: Analogue IC design is especially suited for the implementation of nonlinear signal processing systems because several nonlinearities can be easily implemented in the analogue domain by using physical phenomena as computational primitives. This leads to smaller area, higher processing speed, and lower power consumption compared to a digital implementation of the same nonlinearity. However, these advantages are at the expense of accuracy. We present an analogue nonlinear system which can be used for eigenvalue computation and sorting. Applications for such a system can be found in real-time speech and image processing.

There appears to be no previous work on the analogue VLSI implementation of eigenvalue computation. Most of the implementations of sorting in the analogue domain are based on essentially digital algorithms [1]. In [2], the sorting system is based on isospectral matrix flow, which is a matrix flow in which the eigenvalues of the matrix are preserved. Although the algorithm is essentially analogue, the simulations described in that Paper assume the analogue computing elements to be ideal. This is unrealistic considering the fact that analogue circuits tend to be limited in accuracy, and hence we do not obtain an insight as to how a VLSI implementation of the system would behave. Our system is also based on an isospectral flow, called double bracket matrix flow, and is built at the transistor level. The implementation is continuous time and fully parallel. We first describe the matrix flow and how it can be used for eigenvalue computation and sorting.

Double bracket matrix flow: The double bracket matrix flow is described by the following matrix nonlinear differential equation:

$$\dot{H} = [H, [H, N]] \qquad (1)$$

where $H, N \in R^{n \times n}$ are symmetric matrices, and $[A, B] = AB - BA$. In [3], various properties of the flow have been described. It can be shown that when the flow acts on a symmetric matrix, it causes the diagonalisation of the matrix. The diagonal elements of the resulting matrix are equal to the eigenvalues of $H(0)$ due to the isospectral property of the flow. Thus the system performs eigenvalue computation.

Moreover, if N is diagonal with distinct eigenvalues, it can be shown that the only stable equilibria of the flow are those in which the diagonal elements of H and N are similarly ordered. If the matrix N is constructed so that $N_{11} < N_{22} < ... < N_{nn}$ then, once H is diagonalised, its diagonal entries will be ordered so that $H_{11} < H_{22} < ... < H_{nn}$. Because the final $H_{ii}s$ are the eigenvalues of the matrix, the system not only finds the eigenvalues of $H(0)$, it sorts them as well. This system can be used for sorting lists by choosing $H(0)$ to be diagonal and setting the diagonal elements to the unsorted list.

If we have an $n \times n$ real symmetric matrix H, with elements h_{ij} (where $i, j = 1, 2, ...n$), that is to be diagonalised, and we have a fixed diagonal $n \times n$ real matrix N, with diagonal elements $ni = i$ (where $i = 1, 2, ...n$), then the double bracket flow eqn. 1 can be written as

$$\dot{h}_{ij} = \sum_k h_{ik} h_{kj} (i + j - 2k) \qquad (2)$$

We implement the above equation using analogue integrated circuits.

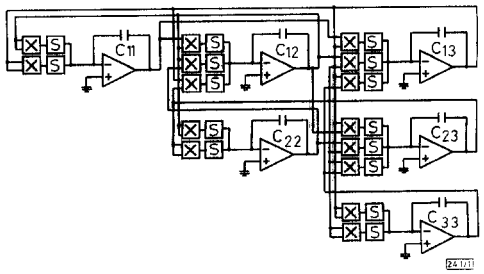

Fig. 1 *Schematic diagram of 3 × 3 system*

×: multipliers
S: scalers

Fully parallel continuous-time analogue system: The simplest and fastest implementation of the system would be to take the fully parallel continuous-time approach, in which we store the value of each h_{ij} in a capacitor C_{ij}, and this value is continuously updated by a current computed using eqn. 2. A schematic diagram of a 3 × 3 system is shown in Fig. 1. For an $n \times n$ system, for the update of each h_{ij}, approximately n parallel multiplications are performed using n multipliers and the summing is performed using an operational amplifier. The scaling by $(i + j - 2k)$ is achieved using two current mirrors in parallel, a p-type current mirror for positive currents and n-type for negative currents. The analogue multiplier is the most crucial computing element in our system. Its size in terms of silicon area limits the size of the matrix that can be diagonalised within a single chip. Therefore, a multiplier with small area is quite desirable. In addition, a multiplier with single ended inputs is better for our system compared to a multiplier with differential inputs because when we use the single ended input multiplier, our system takes up less area and requires less communication between nodes. We could not find a multiplier with the above mentioned characteristics, and so we developed a new multiplier. The details of the multiplier can be found in [4]. The simulated DC characteristic of the multiplier is shown in Fig. 2*a*.

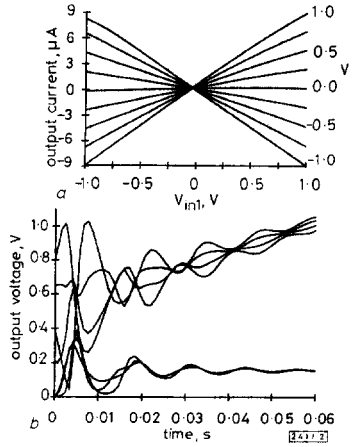

Fig. 2 *Simulated DC characteristics of multiplier and initial output of 4 × 4 system*

a DC characteristics
b Initial output of system

Simulation of 4 × 4 system: We simulated the above system using PSPICE. As an example, we used the system as a sorter. As can be seen in Fig. 2*b*, the flow is unstable. This is because of the offset associated with the multiplier. Because of the offset, δh_{ij} for the diagonal elements is not zero even when the off-diagonal elements reach zero. This causes the diagonal values to move, which in turn makes the off-diagonal values move. This results in the system becoming unstable. By simulation we found that the range of the multiplier must be more than 1000 times the offset for the system to stabilise. Thus for a multiplier with a 10μA range, the output offset must be less than 10nA.

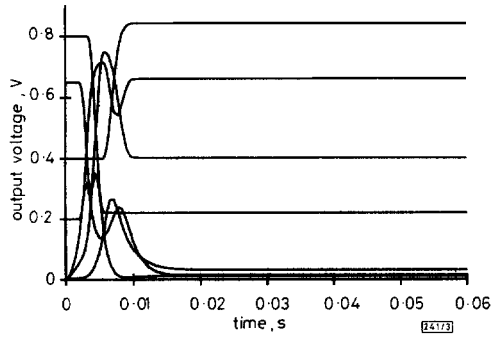

Fig. 3 *Modified output of 4 × 4 system*

This problem can be taken care of by forcing the $\delta h_{ij}s$ of the diagonal nodes to be zero when the output of the off-diagonal nodes is close to zero. In the case of the sorter, we know that the outputs of the diagonal multipliers are always positive because the multipliers are used for squaring. So, for the diagonal nodes, if we

remove the *n*-type current mirror from the scalers and force the offset of the multipliers to be always negative (see [4] on how to adjust the offset of the multiplier), we force the output of the multipliers to go to zero for inputs close to zero. Thus, the output characteristic of such a modified multiplier is similar to the first and second quadrants of Fig. 2*a*, except that the output is zero for inputs near zero. The output of the system using this modification is shown in Fig. 3. The output of the system is stable and the output levels are within 15% of the desired values. In addition, this system is smaller than the unstable system because of the reduced circuitry.

For eigenvalue computation, the output of the multipliers can be positive or negative. We therefore need to construct a multiplier which performs the above mentioned truncation for negative outputs as well. This is achieved by having for each multiplication, a multiplier and an *n*-type current mirror (for the negative outputs), in addition to the multiplier and *p*-type current mirror used above (for positive outputs). This increases the size of the system but makes it stable for eigenvalue computation. The output levels are similar to the sorter, i.e. within 15% of the desired values.

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N. Saxena and J.J. Clark (*Division of Applied Sciences, Harvard Univeristy, Cambridge, MA 02138, USA*)

References

1 LI, J.S.J., and HOLMES, W.H.: 'Analog implementation of median filters for real-time signal processing', *IEEE Trans.*, 1988, **CAS-35**, (8), pp. 1032–1033
2 PAUL, S., and HUPER, K.: 'Analog rank filtering'. Technical University of Munich, Technical Report No. TUMS-LNS-TR-91-21, November 1991
3 BROCKETT, R.W.: 'Dynamical systems that sort lists, diagonalize matrices, and solve linear programming problems', *Linear Algebra and its Applications*, 1991, **146**, pp. 79–91
4 SAXENA, N., and CLARK, J.J.: 'A four-quadrant CMOS analog multiplier for analog neural networks', *IEEE J. Solid-State Circuits*, June 1994, **SC-29**, pp. 746–749

Improved switched-current (SI) bilinear integrator circuit

C. Psychalinos and C.E. Goutis

Indexing terms: Integrating circuits, Switched-current circuits

A bilinear SI integrator circuit with a reduced number of current mirrors is presented. The realisation of the circuit is based on the modification of the corresponding block diagram, to eliminate the required current inversions without delay. The resulting circuit has improved sensitivity performance to current mirror ratio variations.

Introduction: Recently, switched-current (SI) circuits have excited considerable interest in the domain of analogue sampled-data signal processing, due to the compatibility of these circuits with standard digital CMOS process. Furthermore, SI circuits have a low power supply voltage requirement and potential for high frequency operation [1–3]. On the other hand, the accuracy of many SI circuits is quite limited. The main reasons are the ratio-matching accuracy of the current mirror transistors, the clock feedthrough effect, and the finite output impedance of the current sources used in basic SI memory cells [4, 5].

The most widely used design method for high-order SI filters of low sensitivity is the functional simulation of analogue *LC* passive circuits. In this way, the relationships between voltages and currents in the prototype circuit are simulated as transfer functions by SI active circuits. These are then interconnected according to the signal flow graph (SFG) of the *LC* passive prototype [1, 3, 5]. The basic building blocks for functional simulation are SI integrators, inverting and noninverting, with and without damping.

Another way to realise SI filters of high order is the cascade connection of second-order sections (biquads). Using multifeedback structures, the sensitivity of the filters can be reduced. The biquads are realised using two integrators, one inverting and the other noninverting, connected in a feedback loop [1, 5].

The transformation frequently used, between the *s*- and *z*-domains, is the bilinear transformation because of the well known advantages that it exhibits [5]. From the above discussion it is obvious that the bilinear integrator is the basic building block for the realisation of high-order SI filters, and so the quality improvement of integrators has a direct influence on the quality of high-order filters.

The purpose of this Letter is to present a new technique for designing bilinear SI inverting integrator circuits, with reduced sensitivity to current mirror ratio variations. This is achieved after a modification of the block diagram of the integrator, which leads to a reduced number of required current mirrors. The eliminated current mirror is replaced by a single (without mirrored output) current copier cell, in which no mismatch errors can arise [6].

Proposed technique: The proposed technique is based on transfer function modification for some sub-blocks of the integrator, in such a way that the transfer function of the circuit remains unaffected while the total number of required current mirrors is reduced. This is achieved by sharing the delays, which appear in the numerator of the transfer function of some sub-blocks of the integrator, to eliminate the current inversions without delay.

The transfer function of an inverting bilinear SI integrator is the following:

$$H(z) = \frac{I_{out}(z)}{I_{in}(z)} = -K\frac{1+z^{-1}}{1-z^{-1}} \qquad (1)$$

where K is defined by the ratio of the corresponding transistor aspect ratios (W/L). Eqn. 1 can be written as

$$\frac{I_{out}(z)}{I_{in}(z)} = -K\frac{1}{1-z^{-1}} - K\frac{z^{-1}}{1-z^{-1}} \qquad (2)$$

A z-domain block diagram of an inverting bilinear SI integrator is shown in Fig. 1. For the realisation of the term $-K[1/(1-z^{-1})]$, an SI delay cell with feedback is needed. The term $-K[z^{-1}/(1-z^{-1})]$ can be realised by the combination of the same SI delay cell, which in this case produces the term $K[z^{-1}/(1-z^{-1})]$, and an extra current mirror which produces the required current inversion [2, 5, 7]. Note that both current copiers in the SI delay cell must have mirrored outputs in order to perform the scaling operation.

The term $-K[z^{-1}/(1-z^{-1})]$ can be written as

$$\frac{-Kz^{-1}}{1-z^{-1}} = \frac{Kz^{-\frac{1}{2}}}{1-z^{-1}}\left(-z^{-\frac{1}{2}}\right) \qquad (3)$$

From eqn. 3 we find out that the term $K[z^{-1}/(1-z^{-1})]$ can be realised by using same SI delay cell, as in the case of term $K[z^{-1}/(1-z^{-1})]$. The only difference is that we are sampling the corresponding mirrored output of the delay cell, half a period earlier. For the realisation of the term $-z^{-1/2}$ a current copier cell, without mirrored output, is needed.

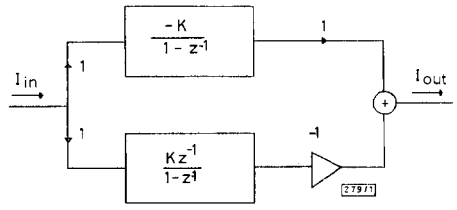

Fig. 1 *z-domain block diagram of an inverting bilinear SI integrator*

In this way, the number of required current mirrors is reduced, and also the sensitivity of the circuit to current mirror ratio variations is reduced. This is due to the fact that, in the single current copier circuit, matching of elements is not required. The block diagram in Fig. 1 can be improved, as shown in Fig. 2.