Local Processing of Sensor Array Data Using Current Mode Circuitry *

James J. Clark
Daniel J. Friedman

Division of Applied Sciences, Harvard University

Abstract

Sensor arrays are capable of generating large amounts of low-level data. Most algorithms which use this data must first perform extensive, repetitive calculations on the data. One way to speed up the system using the sensor data and also to reduce the number of connections between sensors and higher level system elements is to incorporate as much processing power as possible into the sensor chip. We have developed a sensor-processor chip which uses current mode circuitry principles to perform calculations on the sensory data. In the current mode domain, it is straightforward to perform spatial convolutions with fixed and variable kernels. Furthermore, multi-stage convolutions involve identical ideas to those used in the generation of single stage convolutions. Our particular sensor is a split-drain MAGFET; the current division between its two drains varies with magnetic field. All that is required for the application of the ideas presented here to any given sensory system, however, is that the sensor provide a voltage or current output. Regardless of the specific sensor used, then, current mode techniques provide a method for carrying out local processing tasks without using a prohibitive amount of chip area.

1 Introduction

The integration of sensor technology and information processing circuitry is a goal which has great importance in implementations of computer vision systems as well as robotic tactile sensing systems. As research in these technologies progresses, it becomes clearer and clearer that preprocessing of sensory data is required before high-level reasoning tasks can be performed based on the data. The necessary preprocessing is generally a set of highly parallel procedures. As a result, standard serial microprocessor-based approaches are not best suited to the preprocessing tasks. One efficient way to accomplish these tasks is to perform them at the sensor level in the same way, qualitatively, that a biological retina processes visual data before sending its output to a more central nervous block. The obvious advantage of this approach is that a computationally intensive but parallel problem can be solved in a parallel format, increasing the speed of the system. Furthermore, local processing of the sensory data implies that less raw data needs to be sent to higher level processors, further contributing to faster system performance and requiring fewer bulky connections between the sensor and the next processing level.

Our goal is to develop monolithic sensor arrays which integrate processing and sensor hardware. In this paper we present a general approach to the problem of sensor-processor integration using current mode circuitry. We also describe a specific system in which our approach has been used. First we present a brief outline of current mode circuitry operation and how such circuitry can be used to perform several basic functions. We then discuss higher level functions which can be generated from the more basic ones. Finally, we describe a CMOS magnetic field sensor-based circuit which applies the sensor-processor integration idea to robotic tactile sensing.

2 Circuit Theory

The underlying element in current mode circuitry is the current mirror. As its name suggests, this circuit can produce a copy of a reference current given the proper conditions. Current mirrors work by taking advantage of the fact that current flow through MOSFETs in saturation is approximately constant with respect to changes in V_{ds}, the drain to source voltage. Instead, this current depends on fabrication and design parameters like transistor size and threshold voltage as well as on V_{gs}, the gate to source voltage. Figure 1 depicts a basic n-type current mirror. When

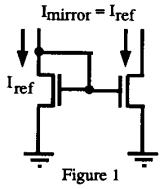

Figure 1

the current mirror is in operation, a reference current flows into the drain of an nFET which has its gate and drain connected to each other. The gate voltage appearing at the gate node will thus correspond to the reference current, rising as the reference current is increased and falling as the reference current is decreased. Provided that the transistor stays in saturation, the gate voltage corresponding to the reference current will remain largely independent of the drain voltage of the right-hand transistor.

Given this gate voltage, it is easy to make copies of a reference current. Considering the equation describing current flow through a MOSFET in saturation provides insights as to how copying and other operations can be performed with current mirror-based circuitry. Recall that for a transistor in saturation,

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2.$$

Recall further that

$$\beta \propto \frac{W}{L}.$$

If the gate voltage generated by the reference current flowing through the gate-drain connected nFET is applied to a transistor with the same β value as the transistor generating the voltage, the current flowing through the second transistor will be the same as that flowing through the first one provided the transistors remain in the saturation regime. In this way, current copies can be obtained. It is also possible to modify the mirrored current by a rational factor by changing the dimensions

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of the transistor through which the mirrored current flows. Transistors with larger $\frac{W}{L}$ values will pass more current for a given gate voltage than transistors with smaller $\frac{W}{L}$ values and so forth.

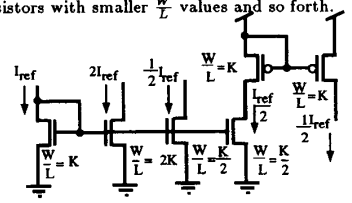

Figure 2: simple inversion.

Another desirable arithmetic operation which can be performed using current mode circuitry is negation. Figure 2 diagrams negation in the current mode circuitry domain. In terms of currents, negation is equivalent to converting a current being sunk by a transistor into one being sourced by a transistor or vice versa. This operation is equivalent to changing current flowing through an nFET to current flowing through a pFET and vice versa. An n-type current mirror output stage (here a single transistor) is connected to the drain of a p-type current mirror input stage. The current flowing through the original n-type current mirror input stage is mirrored by the nFET output stage and hence must also flow through the p-type current mirror. A p-type output stage can be attached to the p-type input stage gate/drain, mirroring the current flowing in the pFET input stage and hence mirroring the current flowing through the nFET input stage. The pFET output stage acts as a current source, however, while the nFET output stage acts as a sink; the current values in the two output stages are thus of the same magnitude but opposite sign.

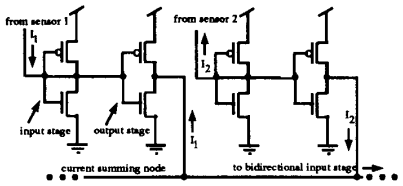

Figure 3: bidirectional current mirrors.

Current mirrors need not take on the exact form described above. Figure 3 depicts two bidirectional current mirrors (1), more flexible incarnations of the standard n-type or p-type current mirror. Note that the input stage of the circuit is actually an n-type and a p-type current mirror input stage connected together. If a reference current is sent into or pulled out of this circuit, the resulting voltage appearing at the gate can be used to create copies of the reference current much as in the case of the current mirror described above. In order for the mirrored current to be able to flow in either direction, however, a slightly more complex output stage is used. Note that this stage is able to source or sink current; its behavior will depend on its gate voltage which will depend on the reference current level. Note first that quiescent currents will flow through the transistors of this type of current mirror independent of the presence of a reference current. If a reference current I_1 is applied to the bidirectional current mirror input stage, it will force the establishment of a voltage condition at the input node gate. This voltage will allow the input stage to accommodate the extra current of value I_1 flowing into the stage, letting it flow out through the nFET of the input stage. This voltage is also applied to the output stage. If the input and output stage transistors have the same dimensions and are in saturation, the fact that they share gate voltages will cause the output stage current behavior to mimic the input stage current behavior. This implies that an extra current of value I_1 will flow through the nFET in addition to the output stage quiescent current. This extra current will come from the current summing bus, a line ultimately connected to the input stage of another bidirectional half current mirror. The sensor and the current summing line both serve as current sources in the situation described above.

The mathematical operations which can be performed with simple current mirrors can also be performed with these more complex current mirrors. Transistor sizing still serves to provide multiplicative factors, although now the nFETs and pFETs must be sized in tandem, taking mobility differences into account when choosing sizes. Inversion of currents is also still possible. In the basic operation of the bidirectional current mirror, the sensor and the current summing line perform the same operation, namely, sinking or sourcing current. A circuit which inverts this relationship is shown in figure 4. A full bidirectional current mirror has been interposed between the output of the mirror attached to the sensor and the current summing line. As before, when the sensor is sourcing a current I_1, the intermediate input stage is sourcing a current I_1. The intermediate stage sourcing current for the first output stage is equivalent to it sinking current for the second stage. This implies that the current summing node must also sink a current I_1, the opposite behavior of the sensor stage.

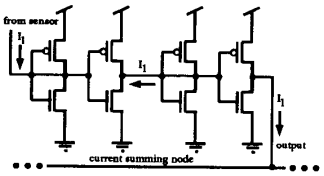

Figure 4: current mode inversion.

Given the flexible versions of sensor signals which can be generated using current mode circuitry, the next step in current mode computation is the combination of those versions. The easy way to add currents is to send them all to a summing node; the output of the system is the current either sunk or sourced by the system. If, however, yet another input stage of a bidirectional current mirror is attached to the summing node, the current output can be turned into a voltage. Provided the input currents do not drive either FET of this final current mirror into saturation, the output voltage as a function of input current remains fairly linear. The voltage form of the output allows the output signal to be copied in the way sensor signals were copied and furthermore is easy to measure and use as the system output.

All the elements are now in place to allow for the generation of weighted sums of sensor-generated current data. Using bidirectional current mirrors, weighted and/or inverted copies of sensor data can be transported to summing nodes all over the sensor array. Essentially, then, it is possible to program spatial convolution with a fixed kernel into the design of a sensor circuit using current mode techniques. The final output of a given cell in a sensor array will be the weighted combination of the raw cell output combined with appropriately weighted copies of outputs from neighboring cells. Furthermore, the output of the current summing part of the system has the same form as the output of any sensor cell. Clearly, then, further stages could be added to the system which use as input first stage processing results. In this format multistage spatial convolutions could be performed locally and in parallel and hence quickly. The output from the combination circuit could then be used either elsewhere on-chip or taken as low-level processed data, the sensor's final output.

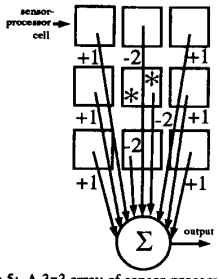

Figure 5: A 3x3 array of sensor-processor cells perform spatial convolution. The starred cell is where the summation occurs and is where the output is available.

An example of the implementation of spatial convolution using current mode circuitry is shown in figure 5. In this situation, the final output

of any given cell has been arbitrarily defined as a function of its own raw data as well as the data of its eight nearest neighbor cells. The spatial convolution, then, is occurring over a 3x3 window. Each cell raw output is the input stage of a bidirectional current mirror. The voltage which is generated at that node is proportional to the sensor current and it is what will be used as data in each of its eight nearest neighbor cells as well as in its own cell. In each case, this voltage is used to make appropriately weighted copies of the sensor output for use by the cells which need the data. In the spatial convolution kernel shown in figure 5, the raw output of the central cell and the raw output of its neighbors above and below is weighted by the factor -2 while the raw output of its remaining neighbors is weighted by the factor +1. The -2 weight is achieved by applying the voltage from the appropriate cell to a bidirectional current inverter and then mirroring the inverter output with a bidirectional current mirror composed of transistors which have $\frac{W}{L}$ ratios which are twice that of the mirror which originally copied the sensor current. The +1 weight is achieved simply by applying the voltage from an appropriate neighbor cell to a bidirectional current mirror output stage with the same size as the input stage generating the voltage.

All of the output stages are connected to a current summing node which is attached to a large bidirectional current mirror (it needs to be large because it has to be able to source or sink all the current supplied to it by the output stages). This, then, is the node at which the final voltage output representing the convolution result can be measured. In an array of sensor elements, the circuitry is designed so that each element applies the same convolution window to its neighbors, except in the border regions of the array. A repetitive, and hence well-suited to parallel architecture, computation is made through on-chip hard-wired local processing of the raw sensory data.

3 Implementation

We have developed a sensor system which uses with current mode local processing circuitry like the circuitry described above. The final goal of this project is to devise a tactile sensor for robotics applications. The sensors which provide the raw data are split-drain MAGFETs (2), merely large pFETs with two drains. When no magnetic field is applied to such a device, the two drains split the current from the source equally. When a magnetic field is applied to the device, however, Lorentz force is generated, causing one drain to pass more than half of the current at the expense of the other drain. The output from the sensor, then, is the current flowing through either drain as both will change with magnetic field variations.

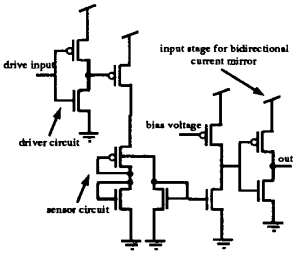

Figure 6: The MAGFET and associated circuitry.

The MAGFET and associated ciruitry appear in Figure 6. In our design, which is currently in the process of being fabricated, the sensors and processing circuitry make up a 3x3 array of sensor-processor units. Figure 9 shows a Magic layout of the array. The convolution kernel we used is the one pictured in figure 5 and described above as an example of how current mode convolution works. This kernel is interesting because it implements a discrete approximation to a second derivative operation on the sensory data. Although the current version of the circuit contains only 9 elements, it is possible to expand the array without a corresponding pinout requirement explosion which could make the devices impractical. One low-pinout requirement expansion approach which we have successfully used and tested in other sensor arrays is to use shift registers to multiplex all similar outputs from sensor-processor cells onto one line (3). As can be seen in figure 7, shift register outputs control the switching of cell outputs onto a global output line. One shift register selects the row from which the output will be taken and a second shift register selects the column, thus pinpointing the sensor-processor cell whose output is active. A different shift register is responsible for turning on a limited number of rows at a time, thus reducing the power used by the system. A reset signal sets some elements high and others low, depending on the particular multiplexing scheme used by the designer. A clock signal then runs the shift registers, causing serial output generation from each sensor element in the array. In a future, larger design using the current mode approach, we will incorporate multiplexing circuitry.

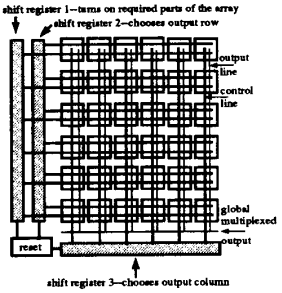

Figure 7: Multiplexed output for sensor arrays.

In a large array, the signal sent by the row-controlling shift register elements would turn on drivers which provide the current which is split between each sensor's two drains. In our current circuit design, all of the driver, input, and output circuits are connected to pins in the IC package. The global current output of the sensor is converted into a voltage in a current mirror and is then mirrored using the input stage for a bidirectional current mirror. The current which is mirrored can be adjusted by changing the bias voltage of the cell. The bidirectional current mirror input is connected to as many bidirectional current mirror output stages as necessary to implement the desired spatial convolution. The output stages are located in the sensor-processor cell where their outputs will be used to calculate a final convolution value. The gate voltages for those stages are provided by associated input stages which are located in the cell which is generating the raw sensor data. As described above, the weights are assigned to each piece of data by transistor sizing in the output stage. One obvious possibility for increasing the flexibility of the array, then, would be to dynamically change weights merely by switching between output stages with different transistor geometries.

Our sensor-processor array will implement a one-stage convolution on a 3x3 spatial kernel. The system performs a +1 -2 +1 filter stacked three high on the array of sensor outputs. Circuit simulation results show that the system will respond as expected given the convolution kernel; it will respond most strongly to magnetic field edges which are oriented so that they are parallel to the boundaries between weight regions. Figure 8 shows the simulated response of the array to a maximal response-inducing stimulus and a stimulus in which the field changes uniformly across the array. Deviations from the expected flat-line response in the uniform field response are reflections of imperfections in weight generation.

4 Conclusions

We have developed a sensor array which performs local processing on sensory data using current mode circuitry. This approach to machine perception solves parallel problems in a parallel format, saving time and connector space. Discrete approximations to spatial convolution operations like low-pass filtering, edge detection, and so forth are easy to generate in the current mode circuitry domain. Multi-stage filtering operations involve the same principles as single stage filtering operations and hence are also straightforward. The current mode domain is a regime in which arithmetic computations on ana-

log data can be performed in proximity to sensor circuitry without using a prohibitive amount of space and is thus a promising area for work in sensor-processor combination and for sensor data processing in general.

5 References

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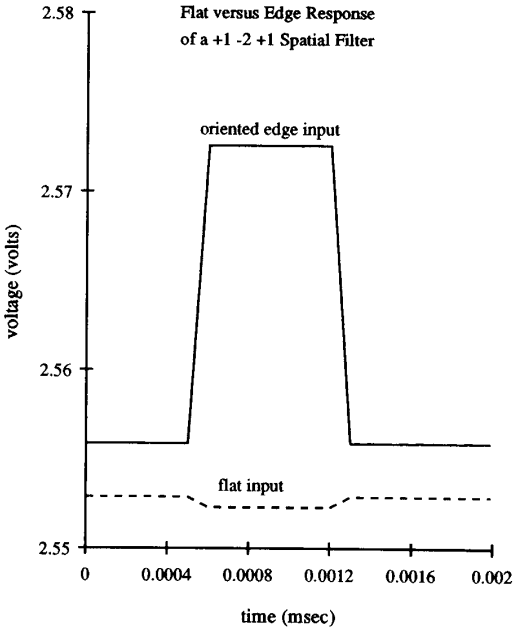

Figure 8: Response of a circuit simulation of a current mode +1 -2 +1 filter to a magnetic field edge as compared to a uniform field increase.

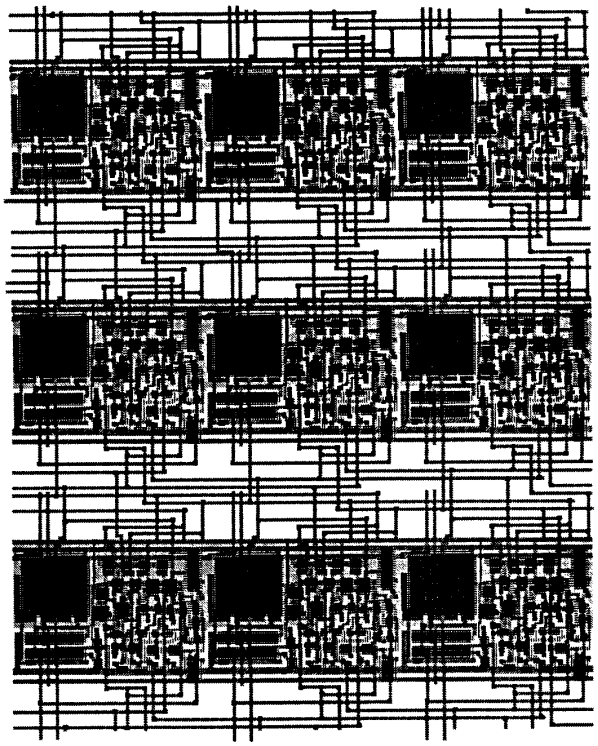

Figure 9: Magic layout of a current mode sensor-processor array now in fabrication.